

FIG. 1

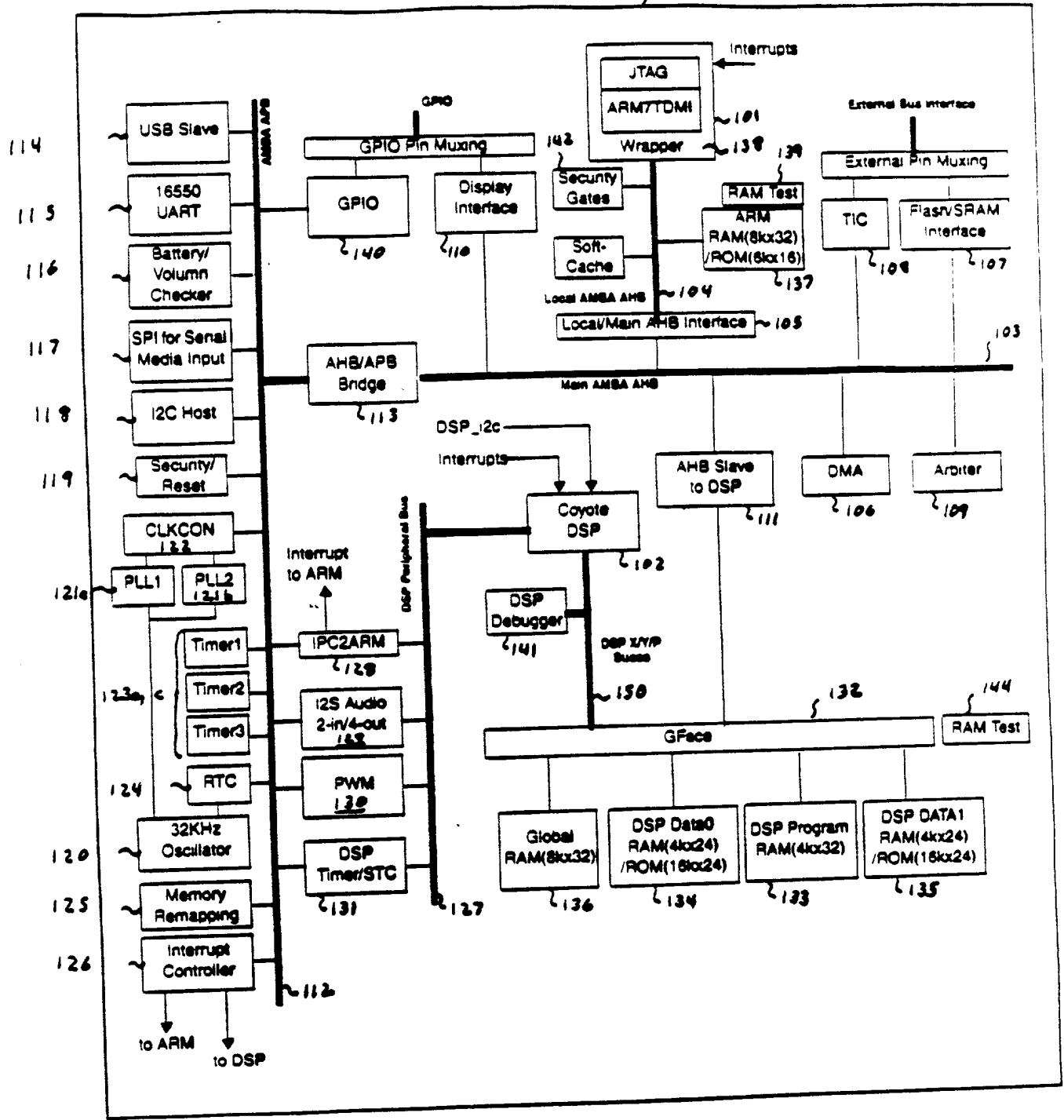
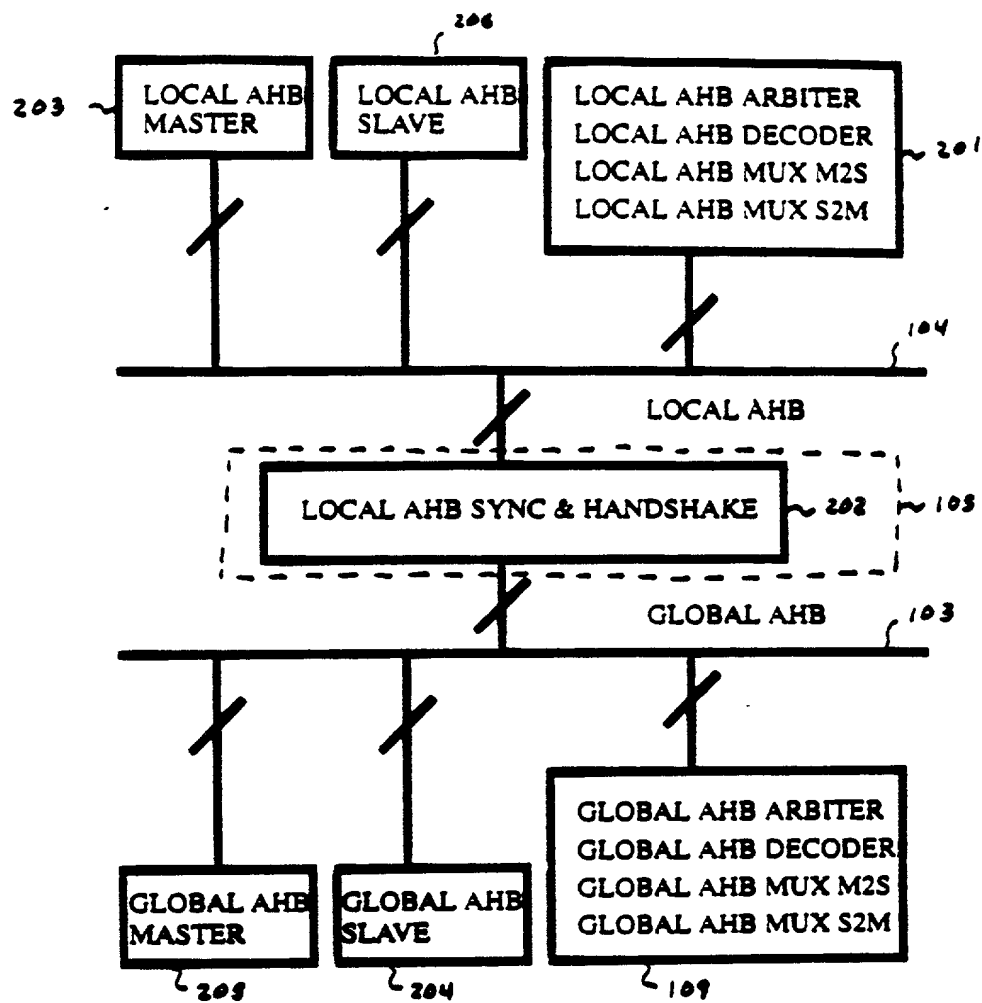


FIG. 2A



The diagram shows the timing of various signals relative to the GHCLK domain. The signals are:

- GHCLK**: Global clock signal.
- LHCLK**: Local clock signal.
- LHADDR**: Local address signal, shown as a sequence of addresses (A0, A1, A2, A3).
- LHTRANS**: Local transfer signal, shown as a sequence of transfer signals (T0, T1, T2, T3).
- LHREADY**: Local ready signal, shown as a sequence of ready signals (R0, R1, R2, R3).
- LRDATA**: Local read data signal, shown as a sequence of data signals (D0, D1, D2, D3).
- LWDATA**: Local write data signal, shown as a sequence of data signals (D0, D1, D2, D3).
- OHADDR**: Output address signal, shown as a sequence of addresses (A0, A1, A2, A3).
- OHREADY**: Output ready signal, shown as a sequence of ready signals (R0, R1, R2, R3).
- ORDATA**: Output read data signal, shown as a sequence of data signals (D0, D1, D2, D3).
- OWDATA**: Output write data signal, shown as a sequence of data signals (D0, D1, D2, D3).
- GHSELaddr**: Global select address signal, shown as a sequence of data signals (D0, D1, D2, D3).
- GHSELaddr_reg**: Global select address register signal, shown as a sequence of data signals (D0, D1, D2, D3).
- LHBUSREQaddr**: Local bus request address signal, shown as a sequence of data signals (D0, D1, D2, D3).
- LHGRANT**: Local grant signal, shown as a sequence of data signals (D0, D1, D2, D3).

FIG. 3B

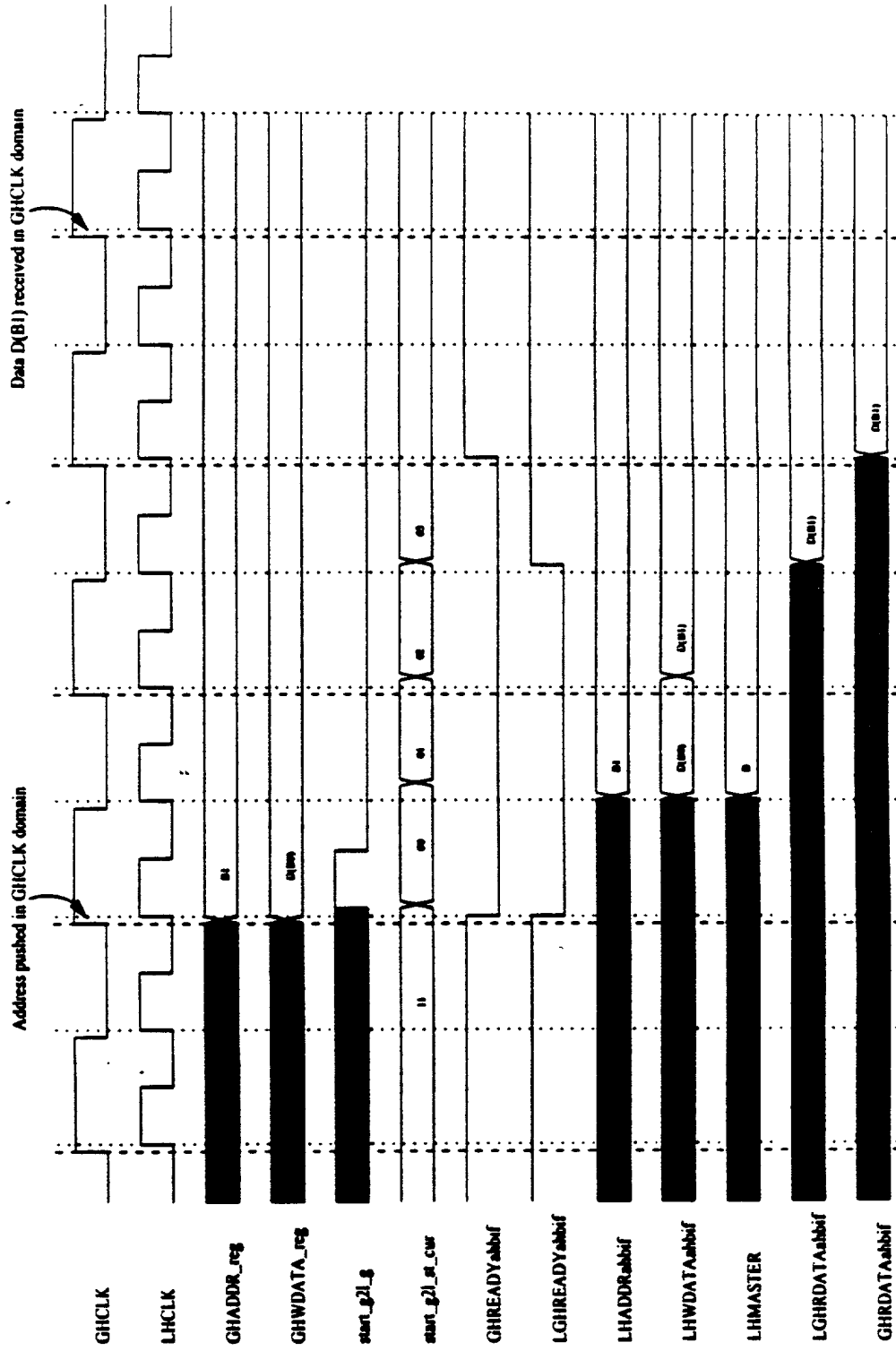
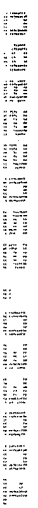


FIG 22C

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FIG. 4B

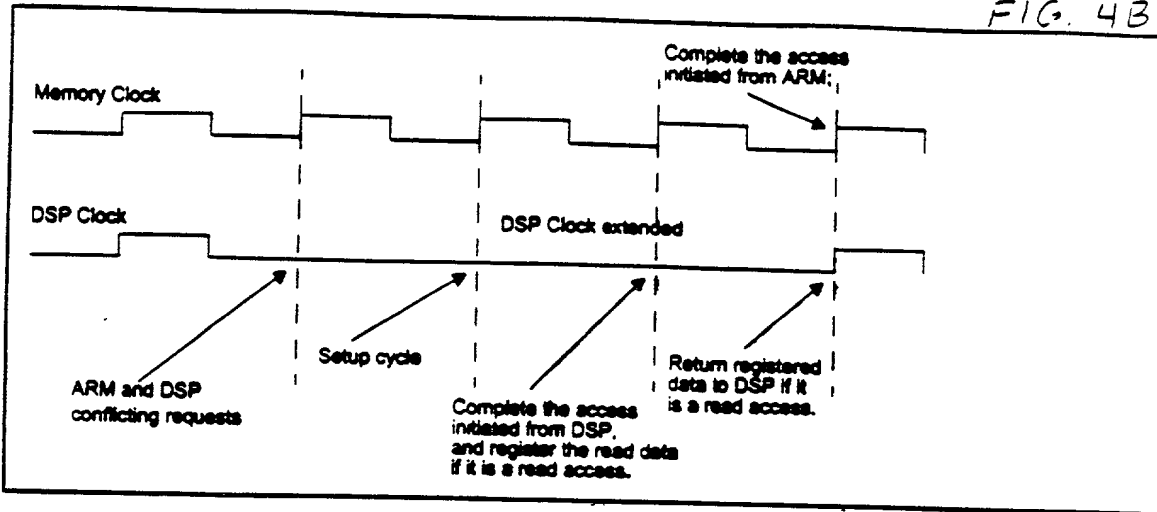
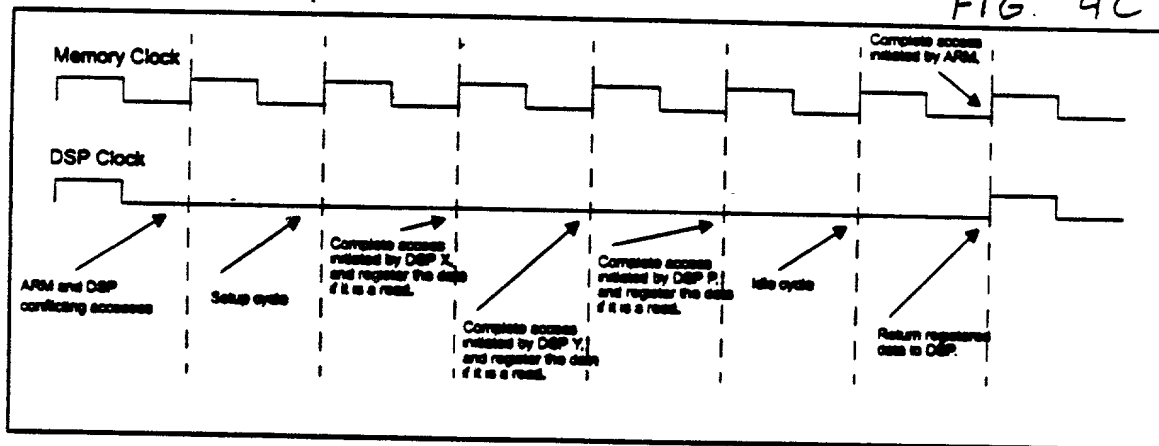
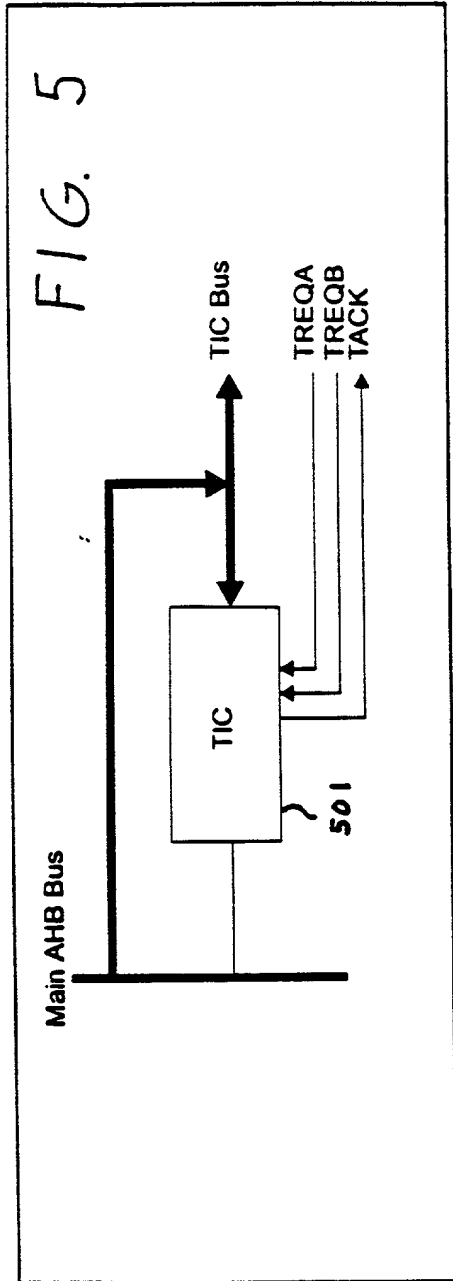
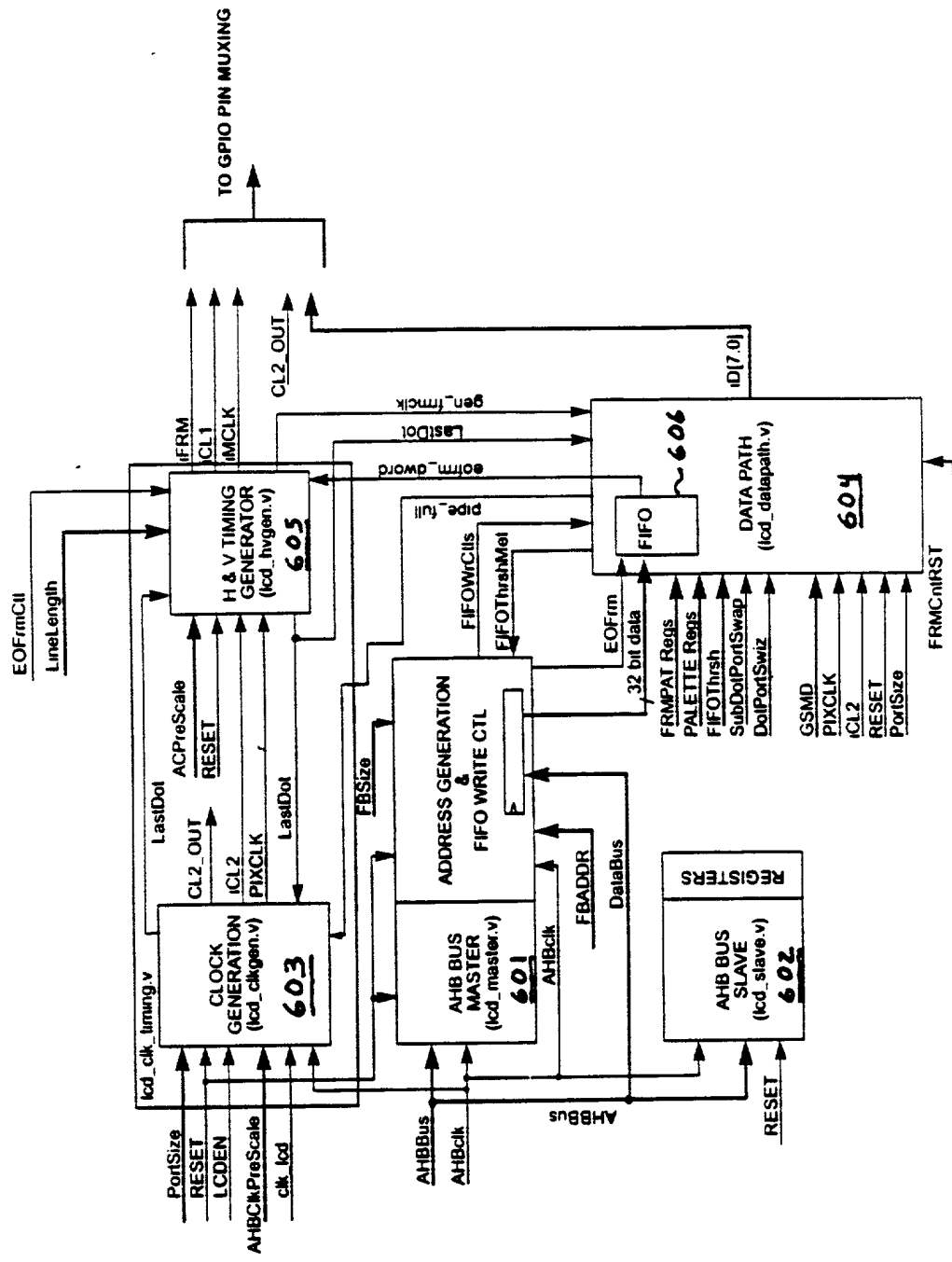


FIG. 4C







LCD Controller (lcd_top.v) Block Diagram

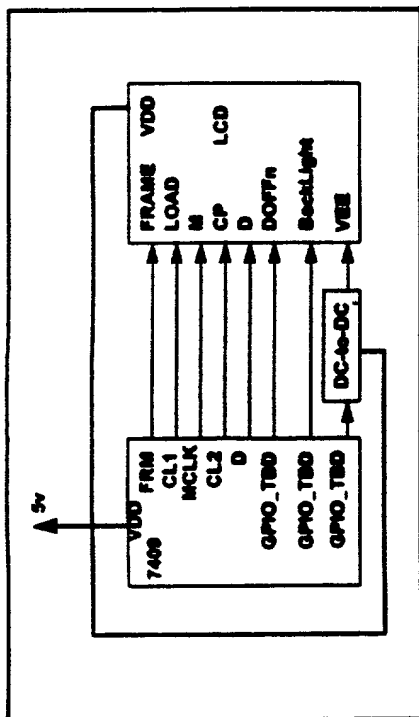


FIG 6B

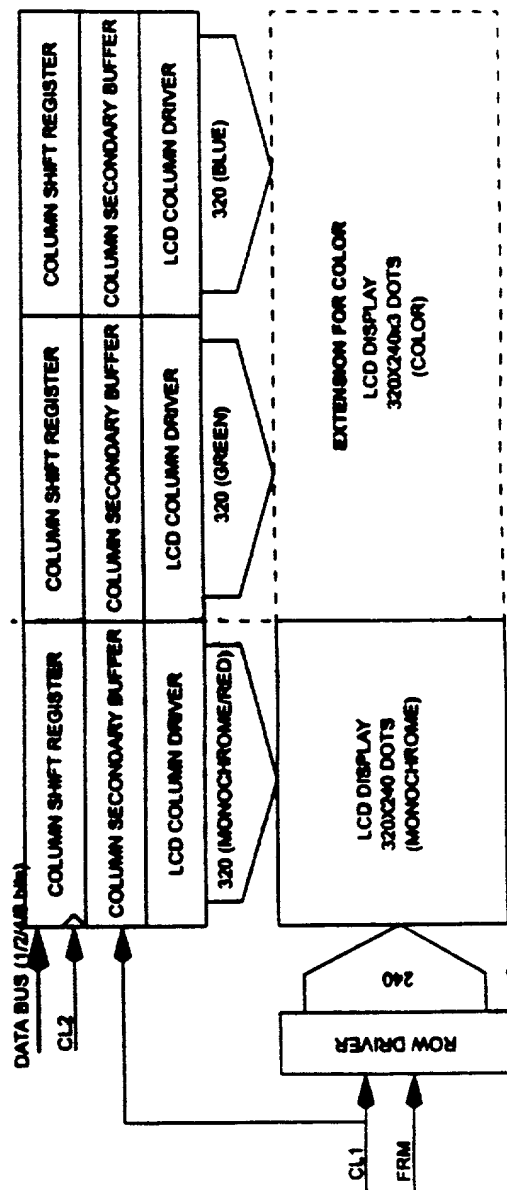


Fig 6c

FIG 6 E

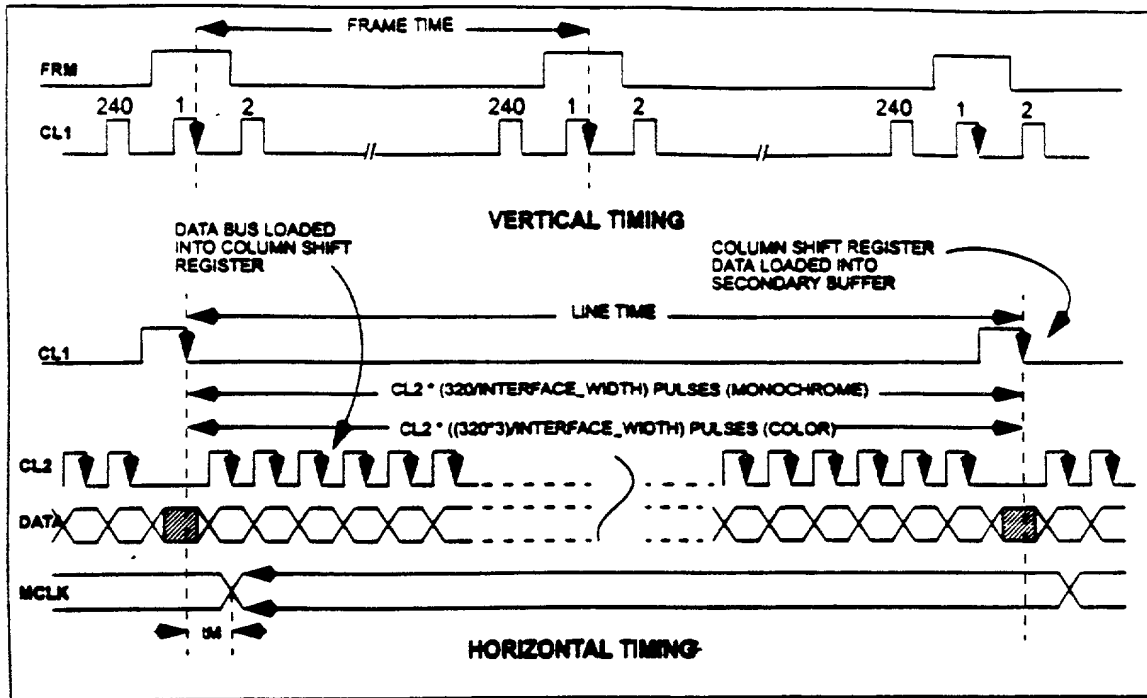
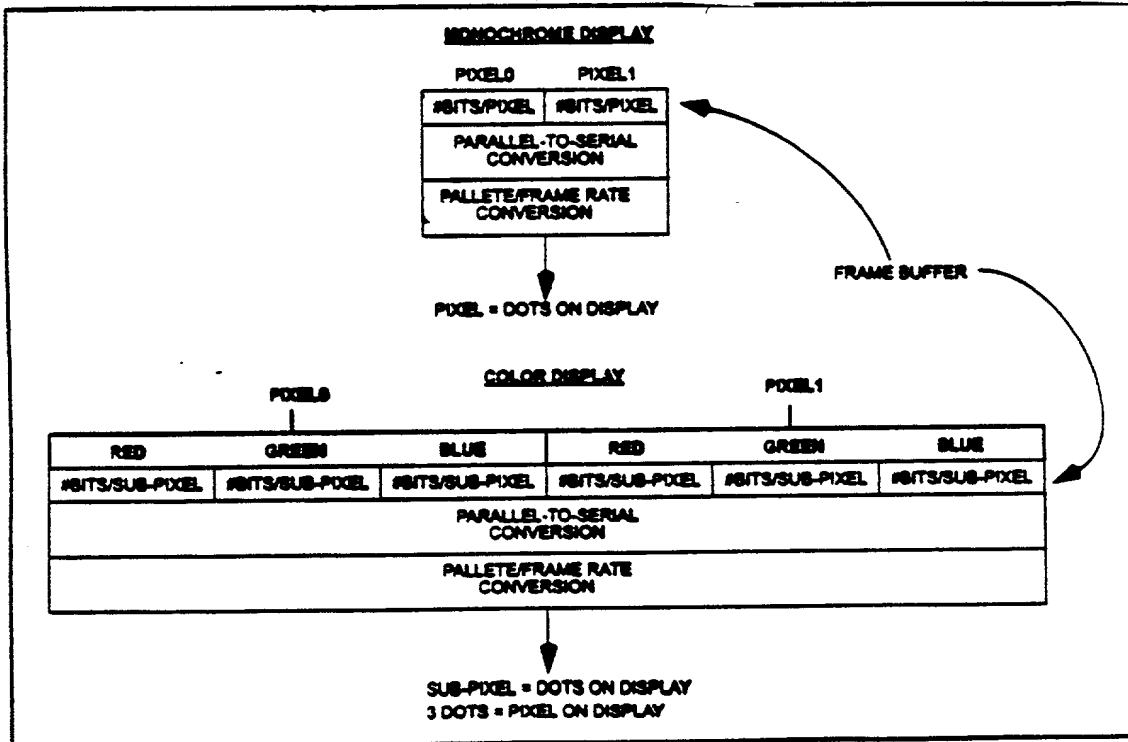


FIG 6 D



4
200

FIG. 6F

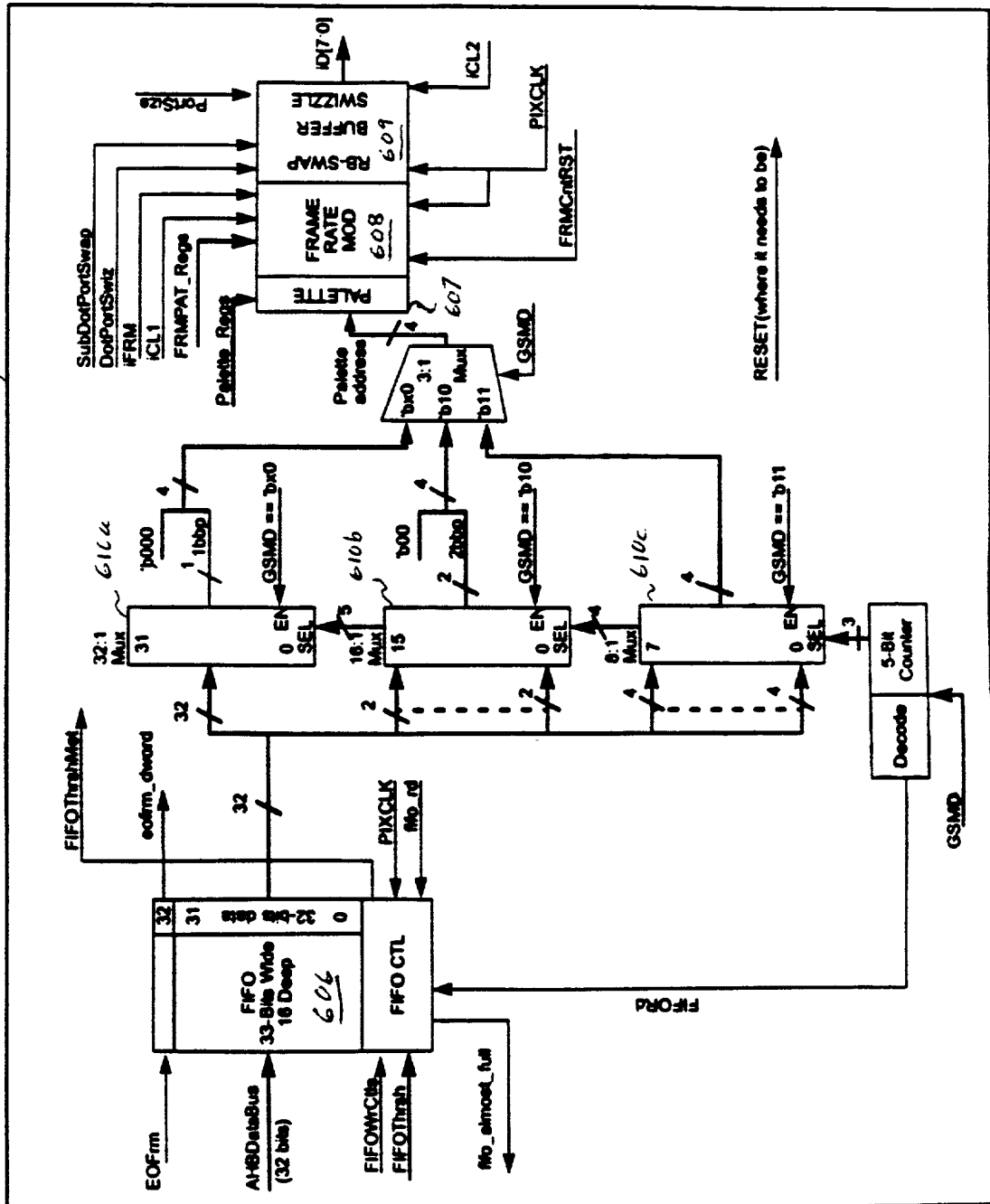


FIG 6G

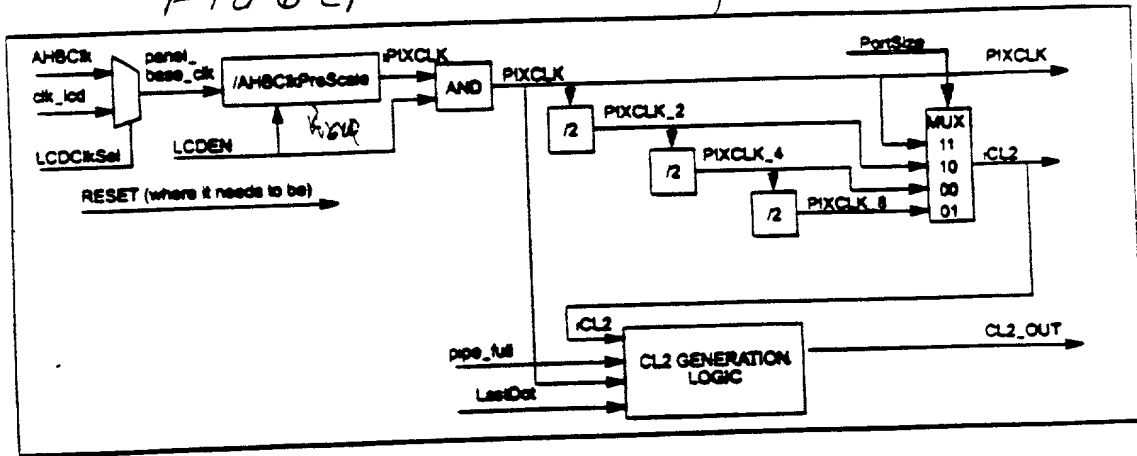


FIG 6H

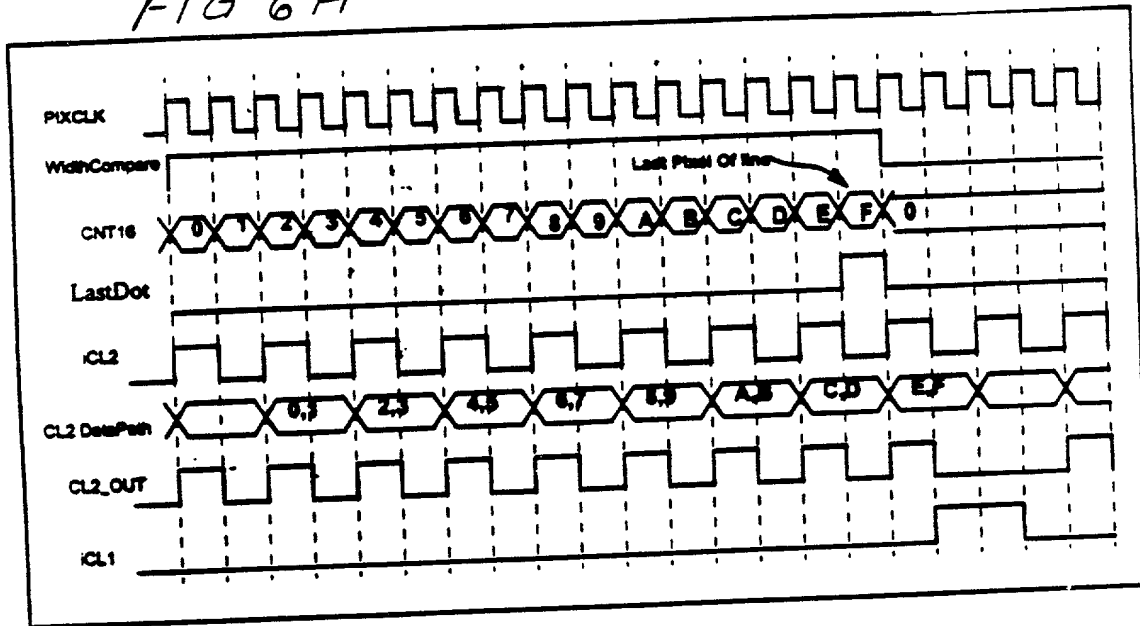


FIG 61

605

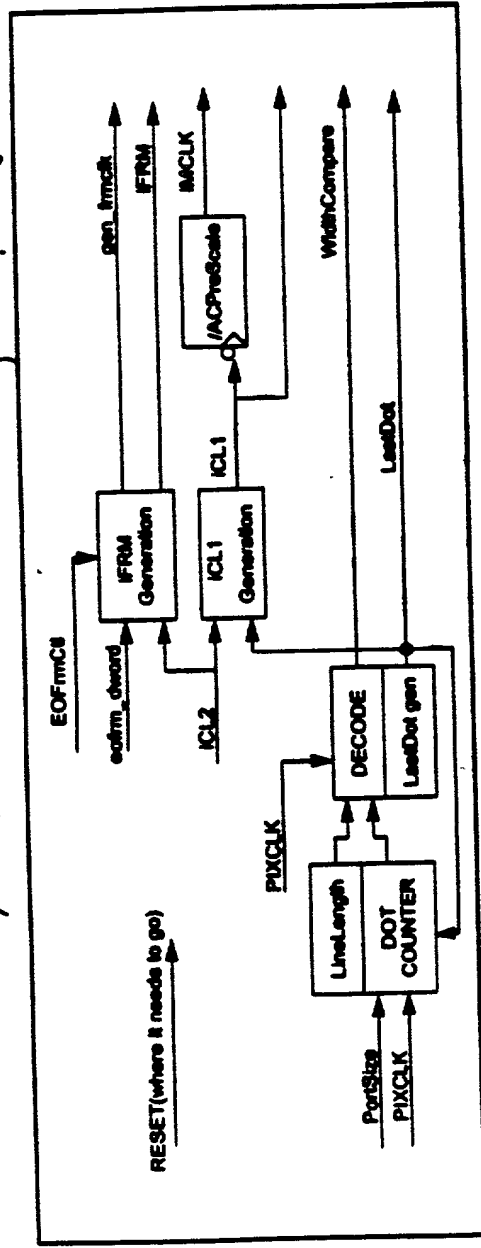


FIG 67

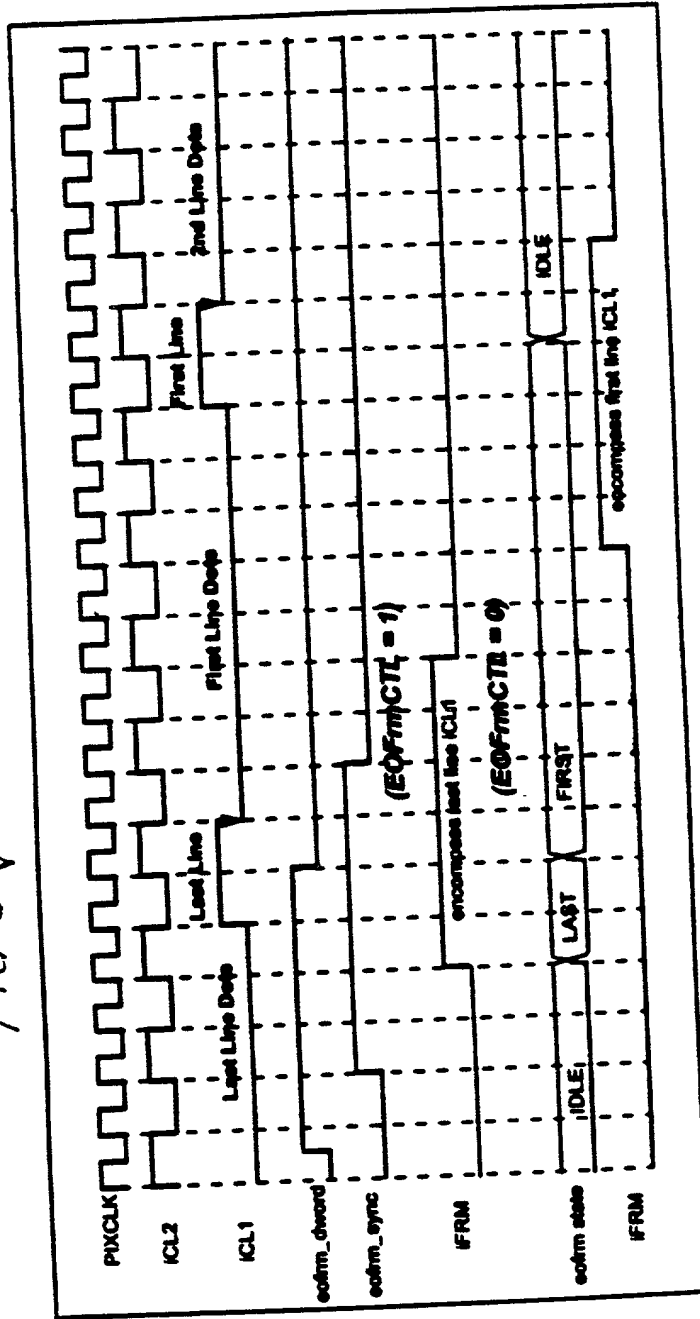


FIG. 6k

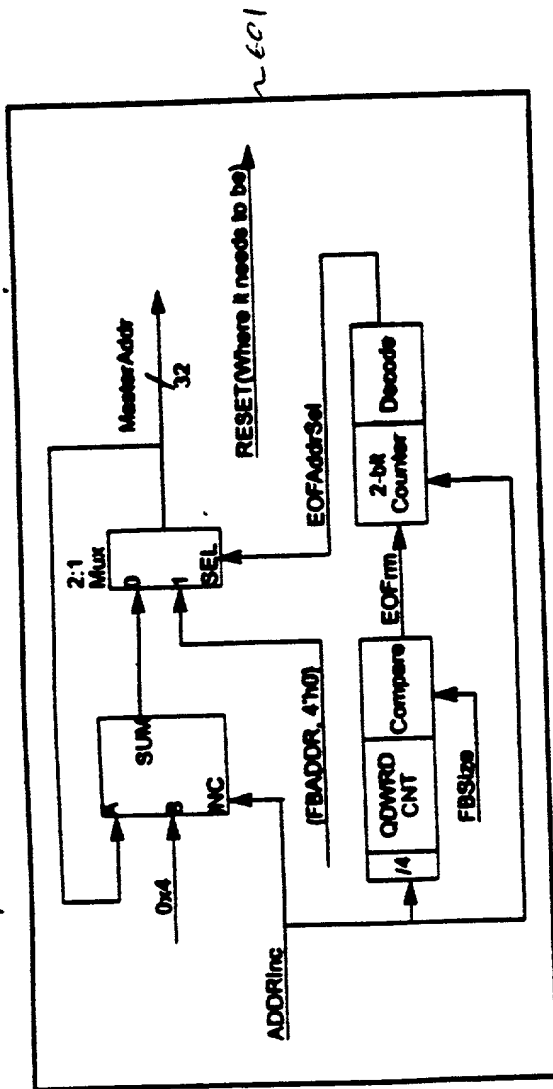


FIG 6L

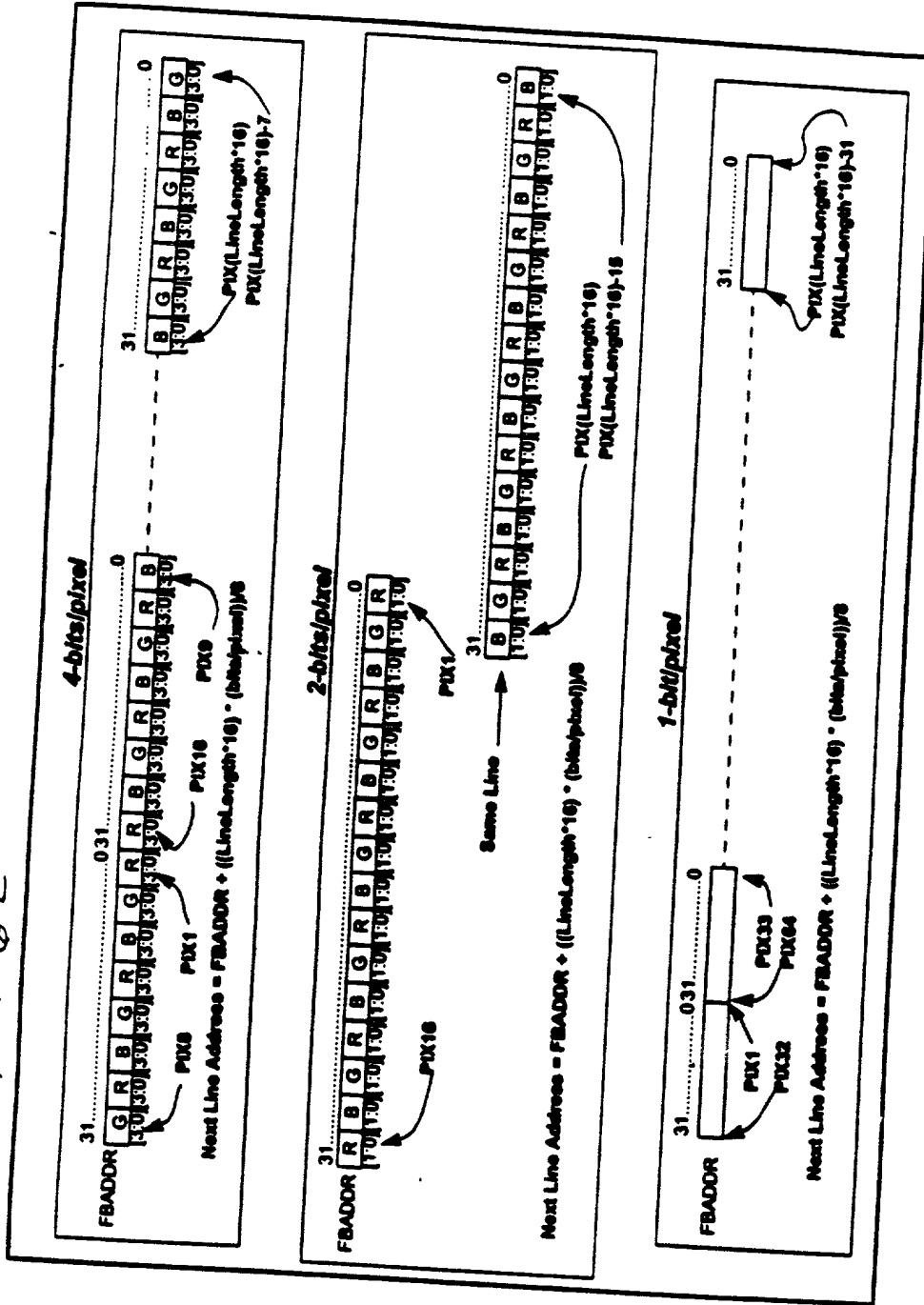


FIG 6M

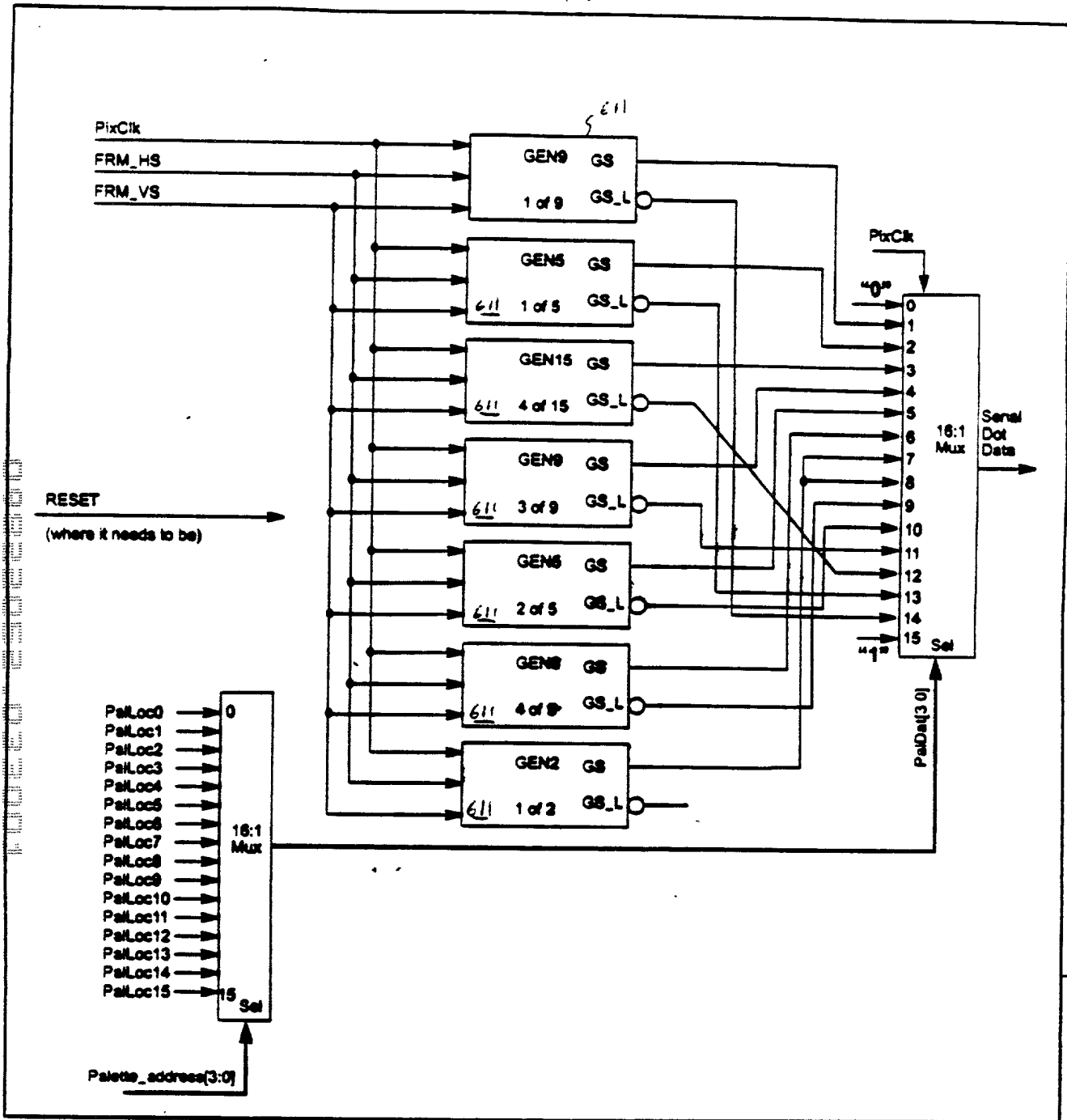
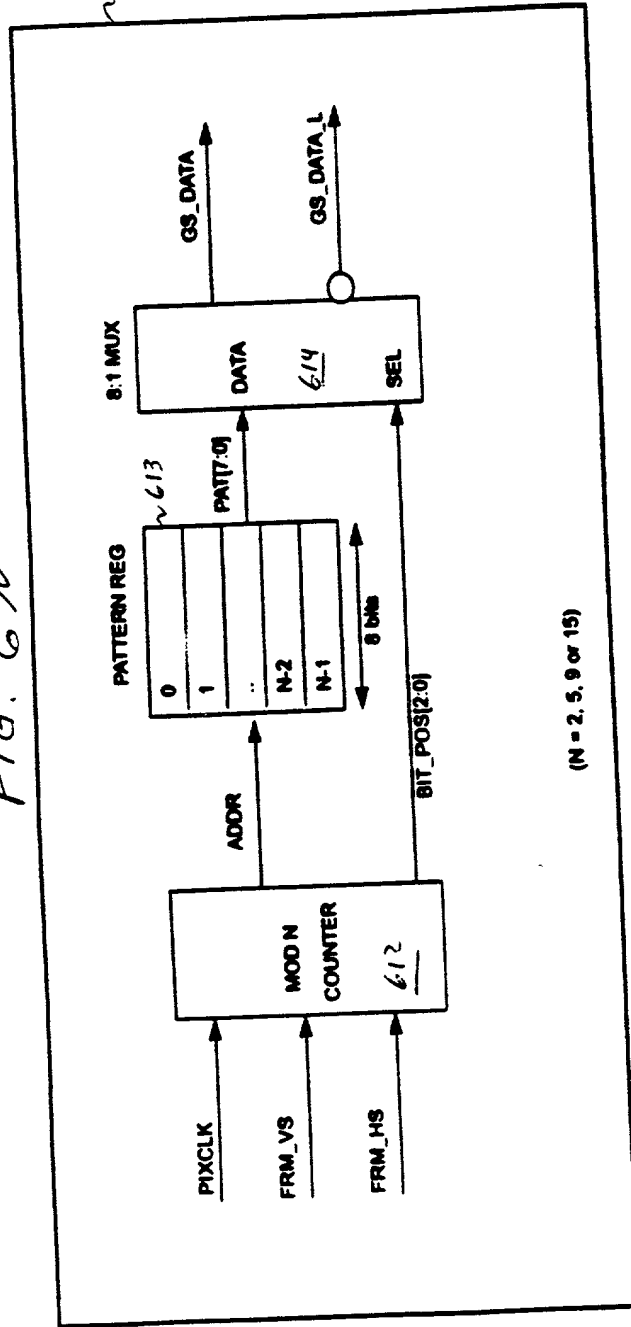


FIG. 6N



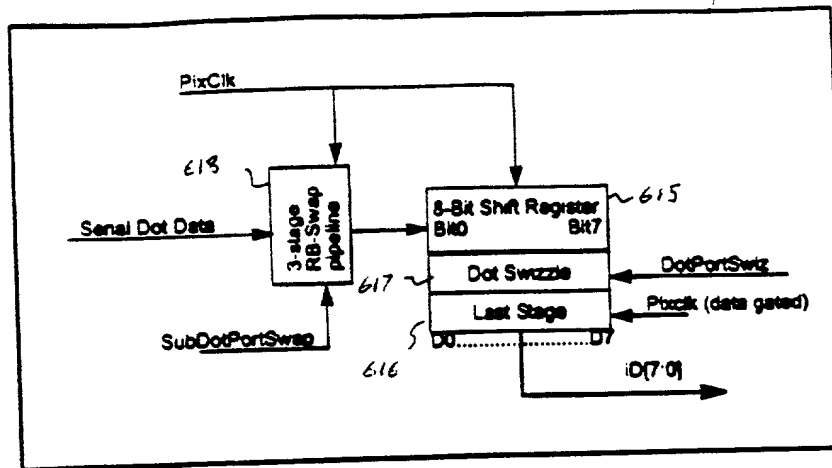
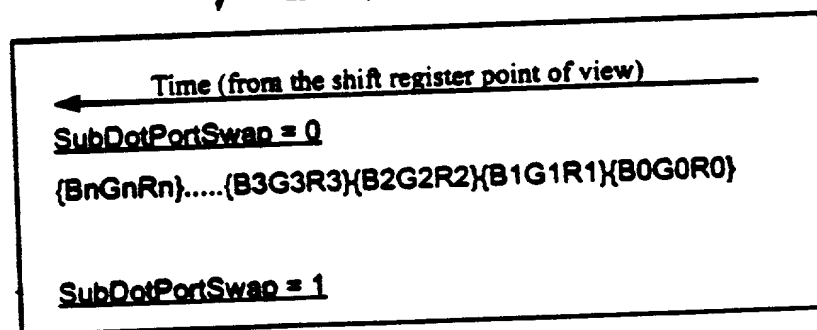


FIG 60

FIG. 6P



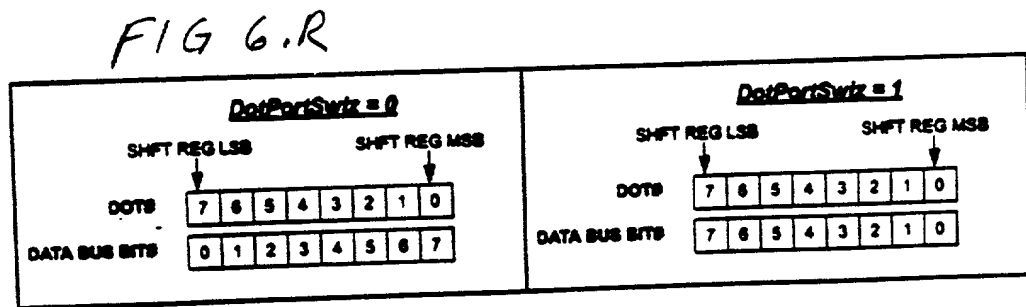
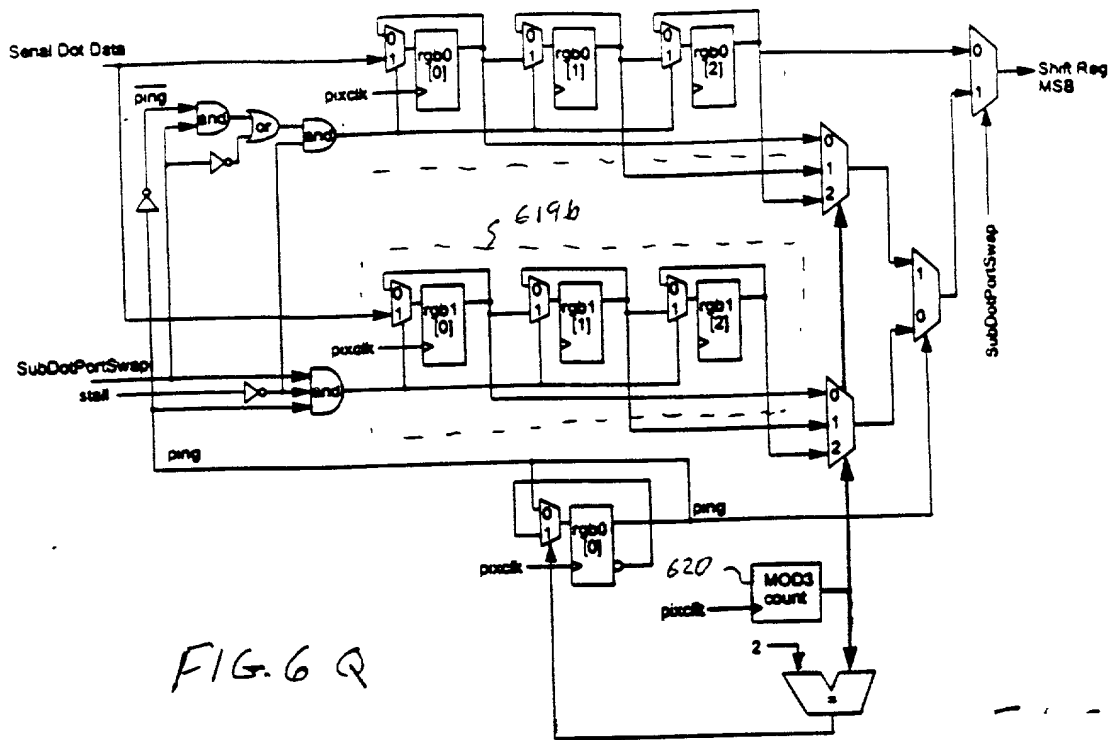
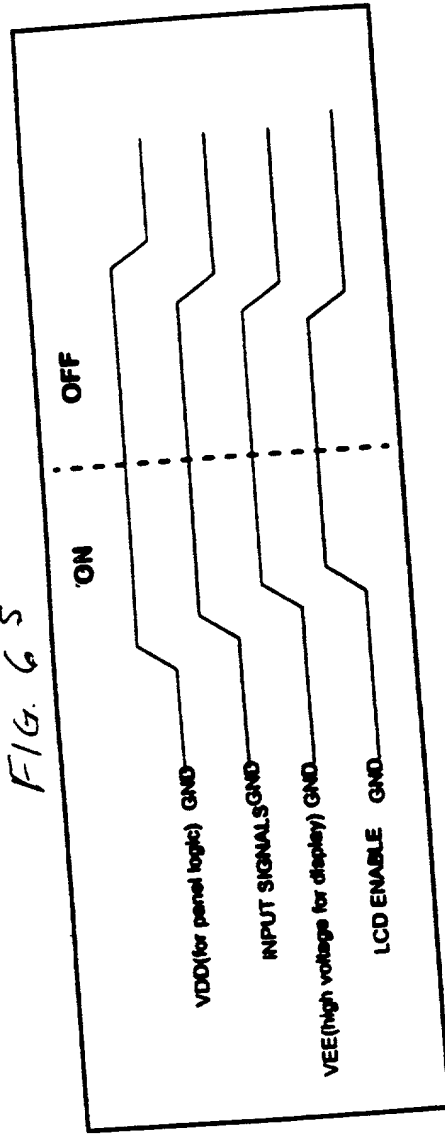


FIG. 6 S



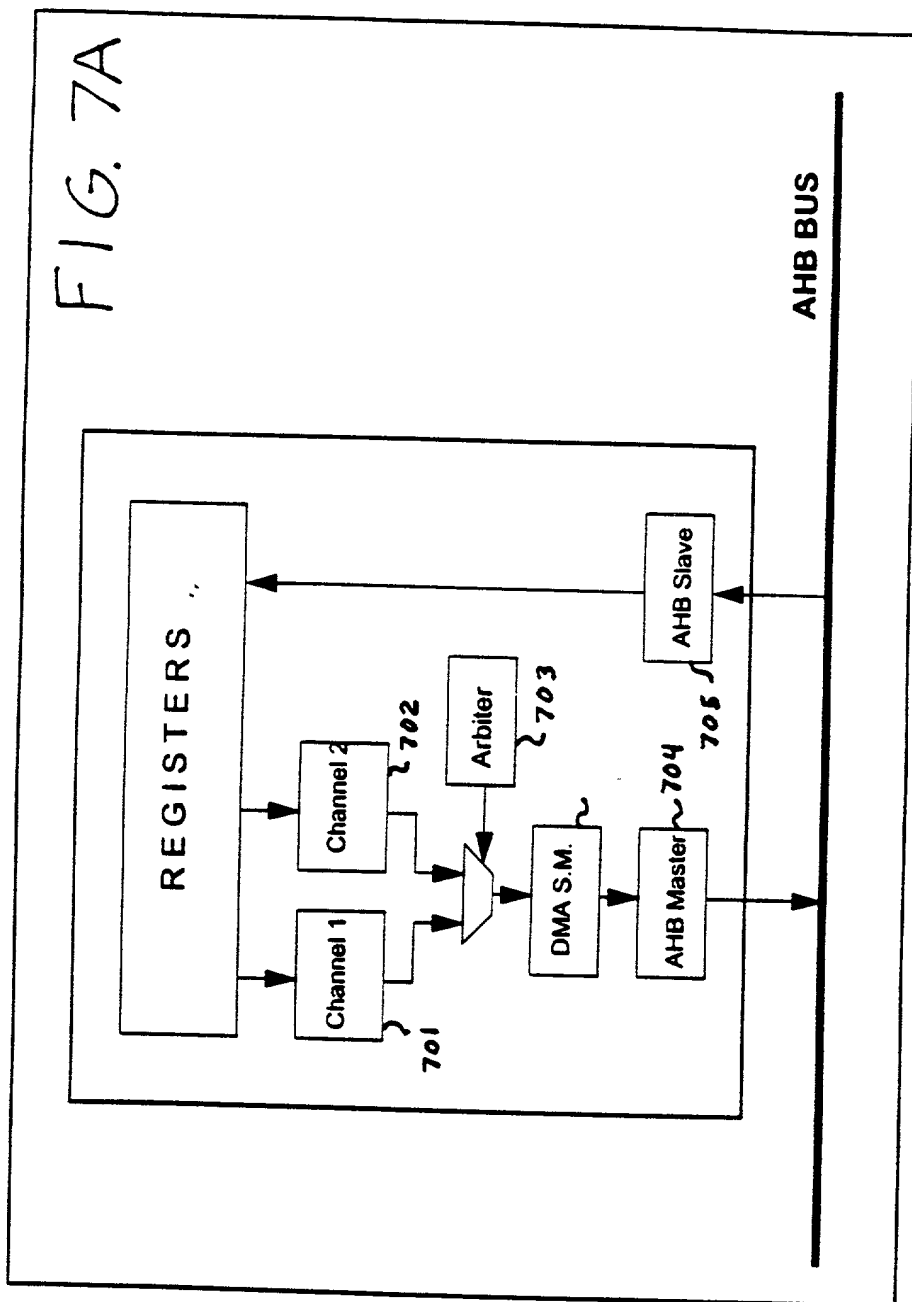


FIG. 7B

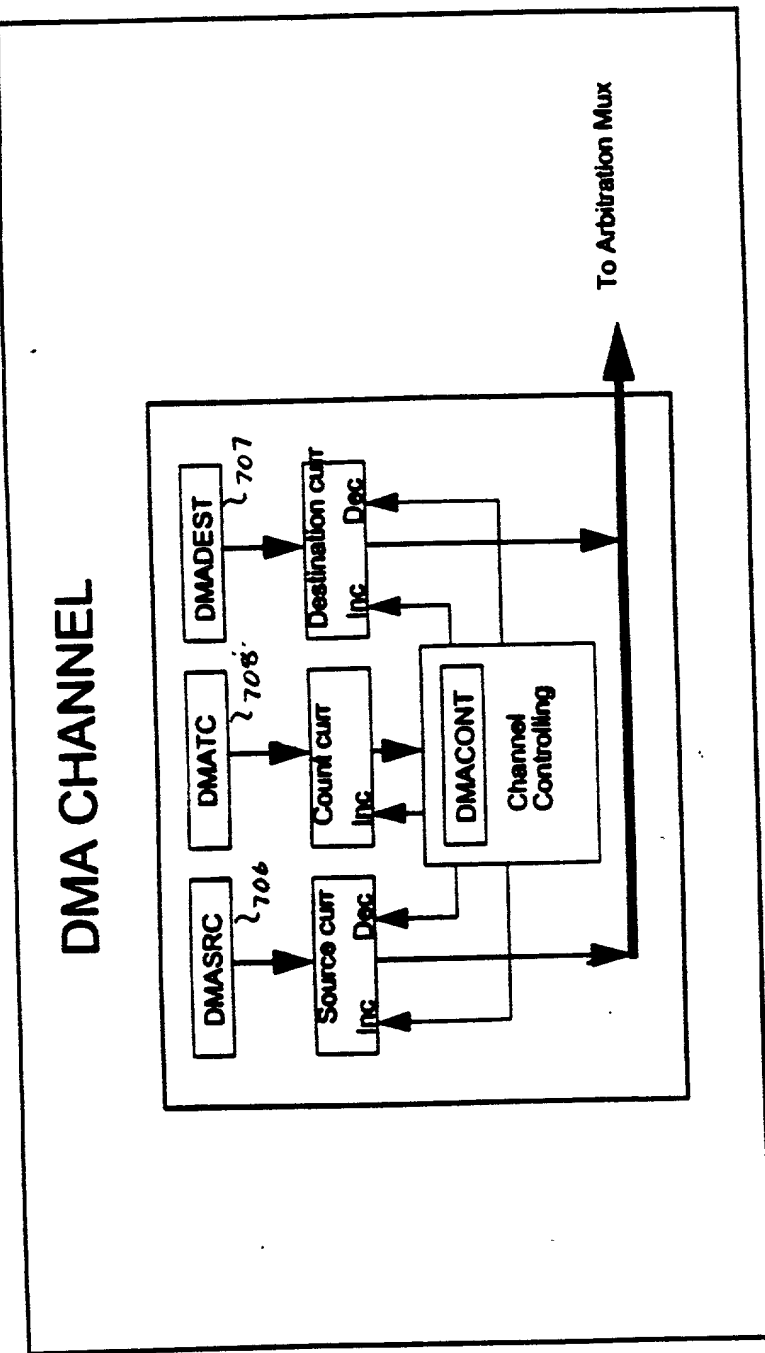
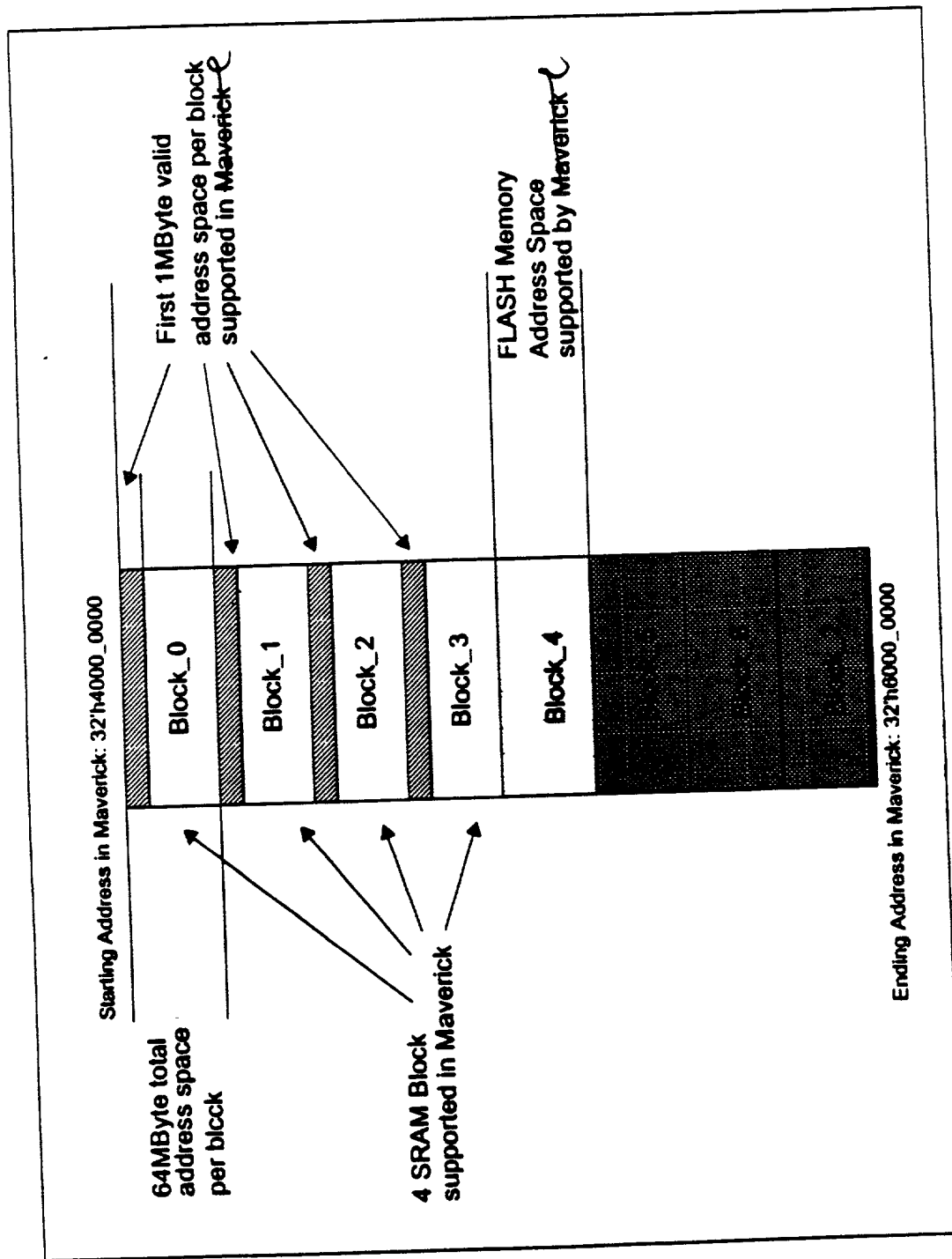


FIG. 8





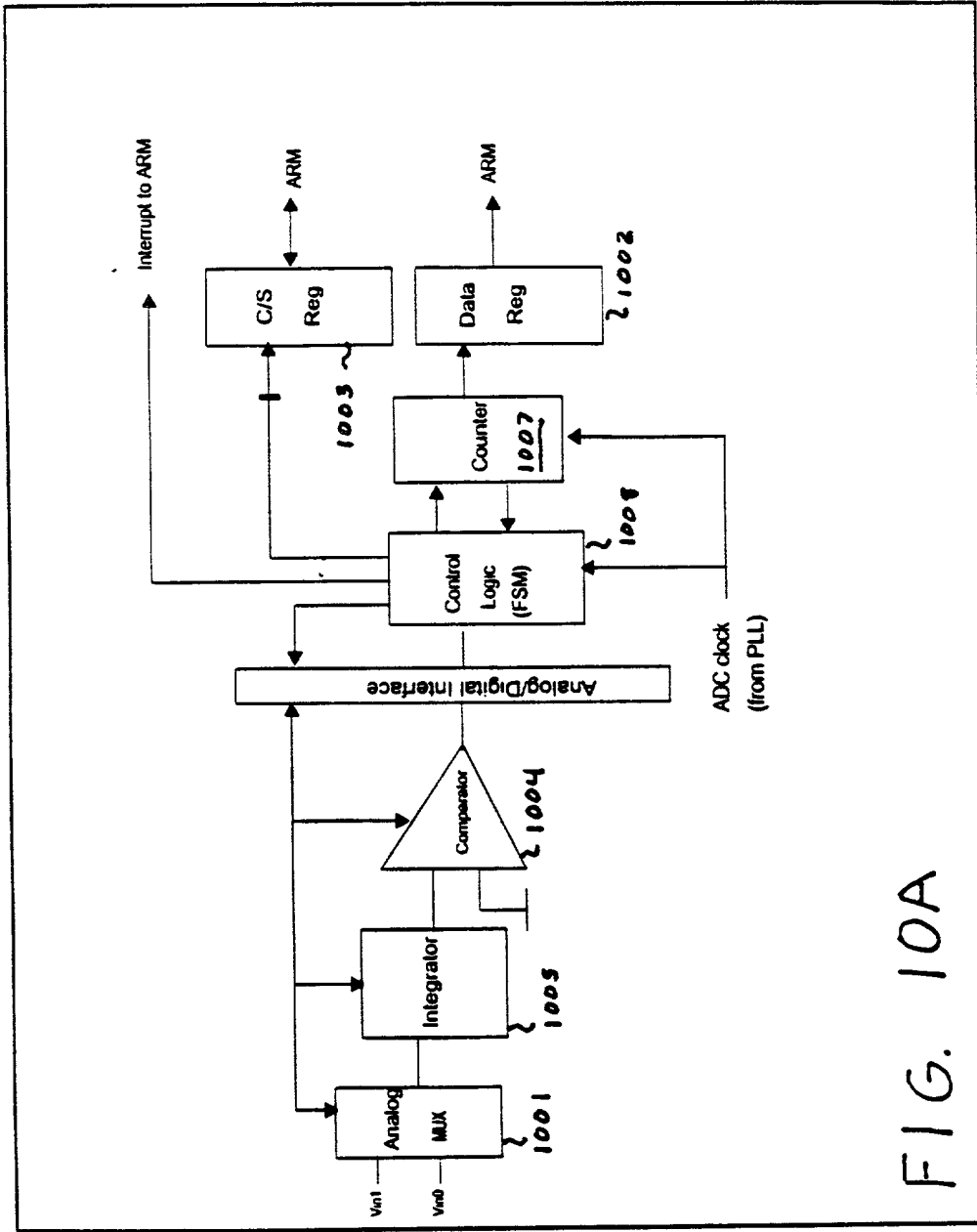


FIG. 10A

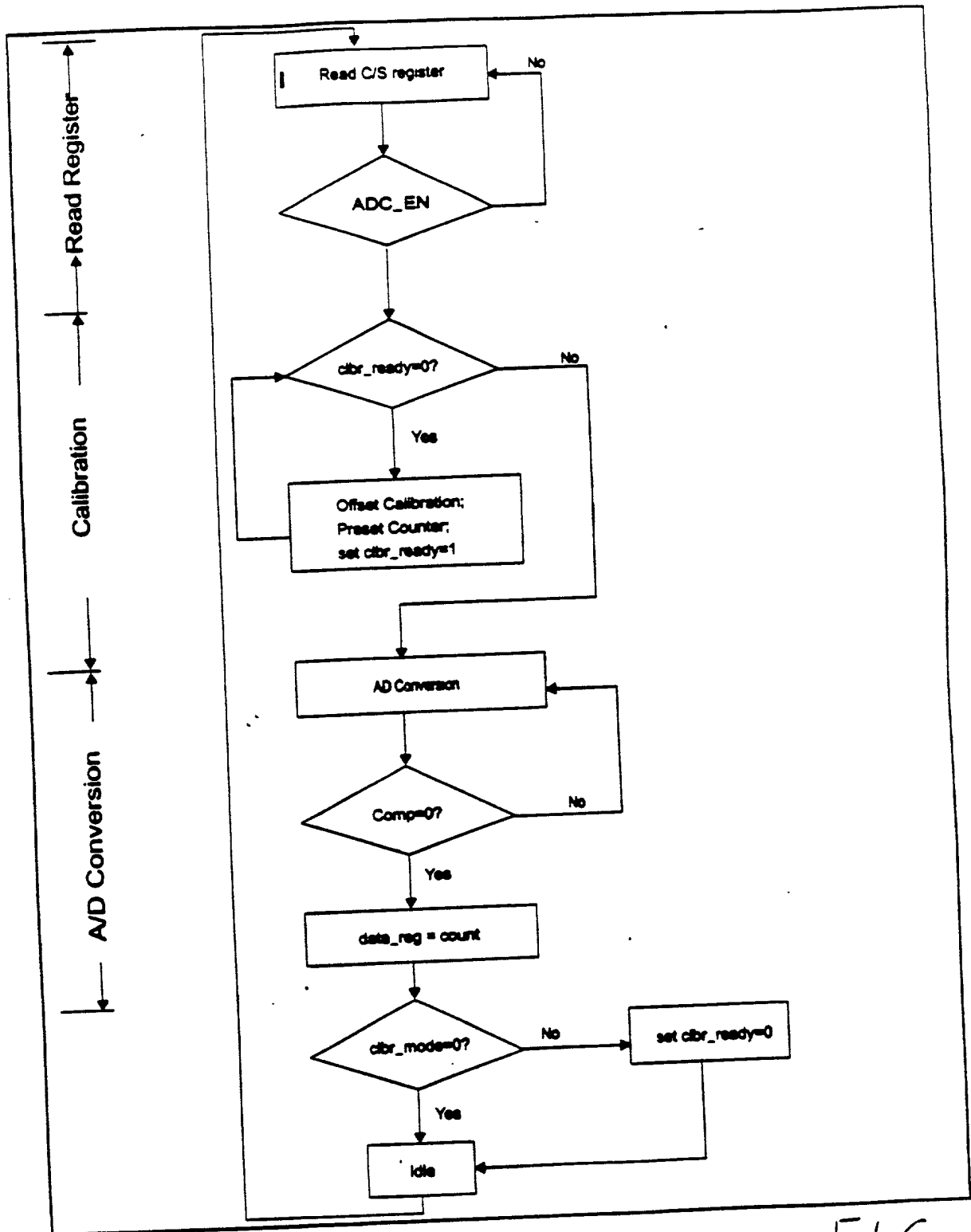


FIG. 10B

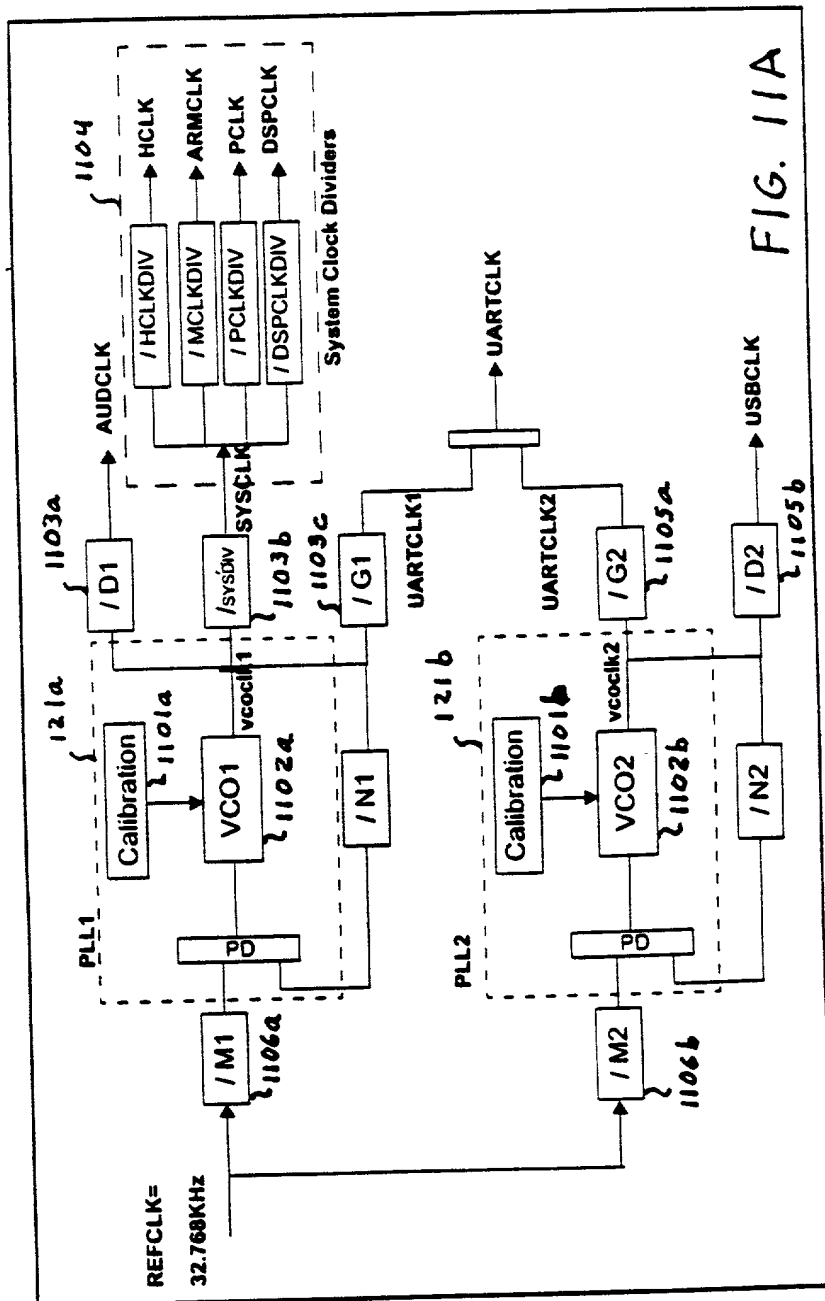


FIG. 11A

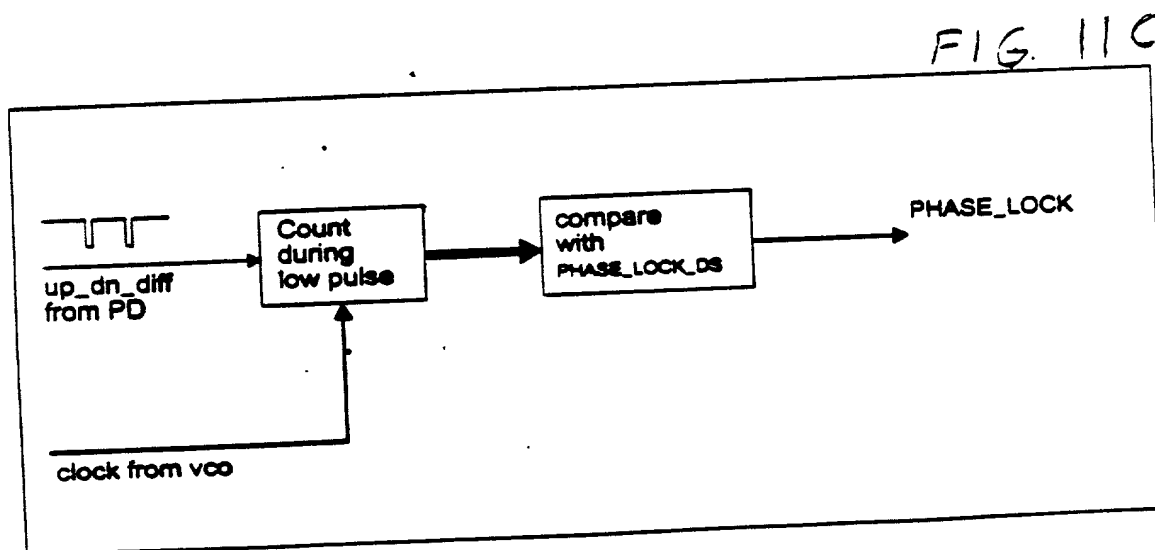
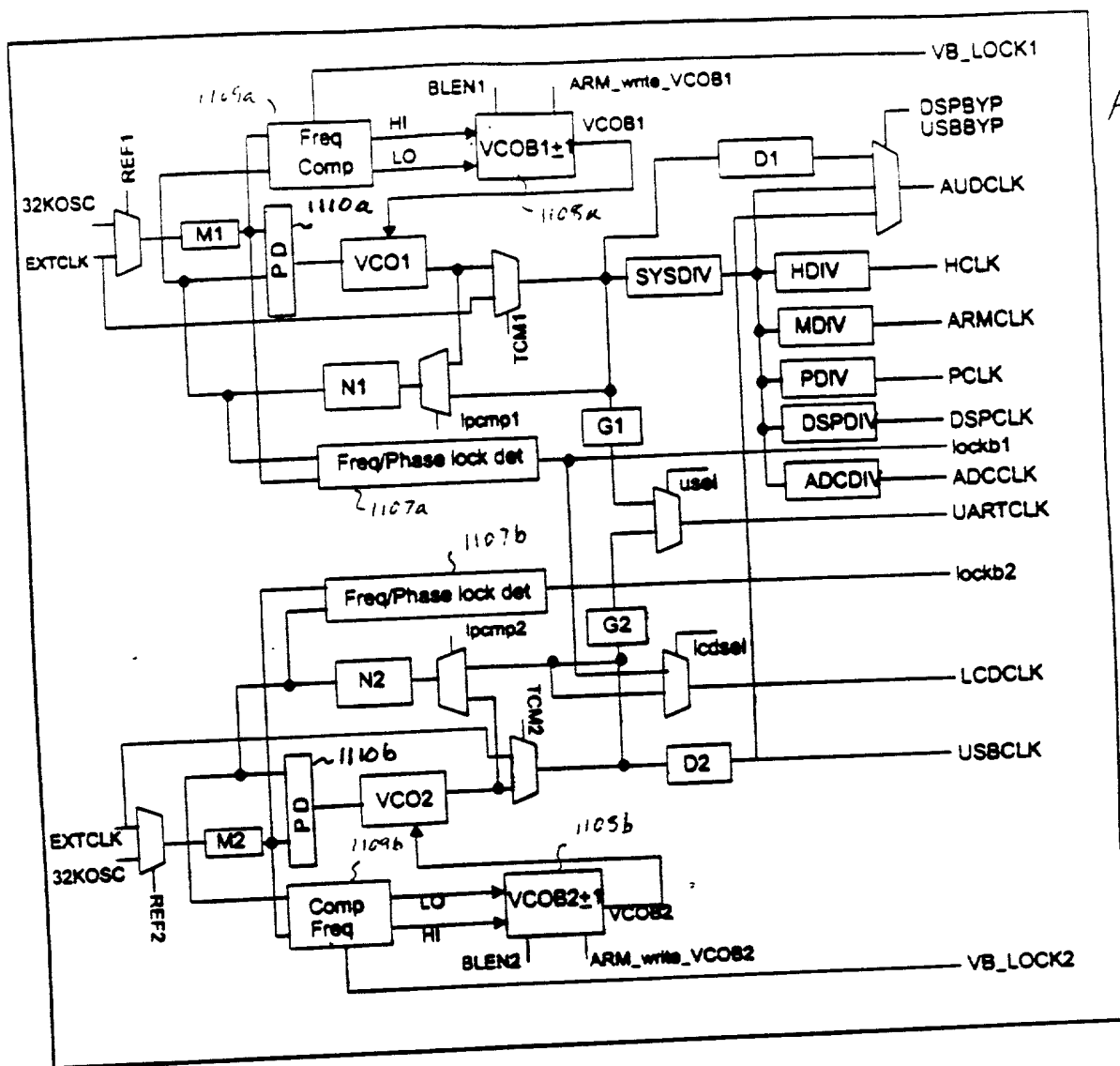
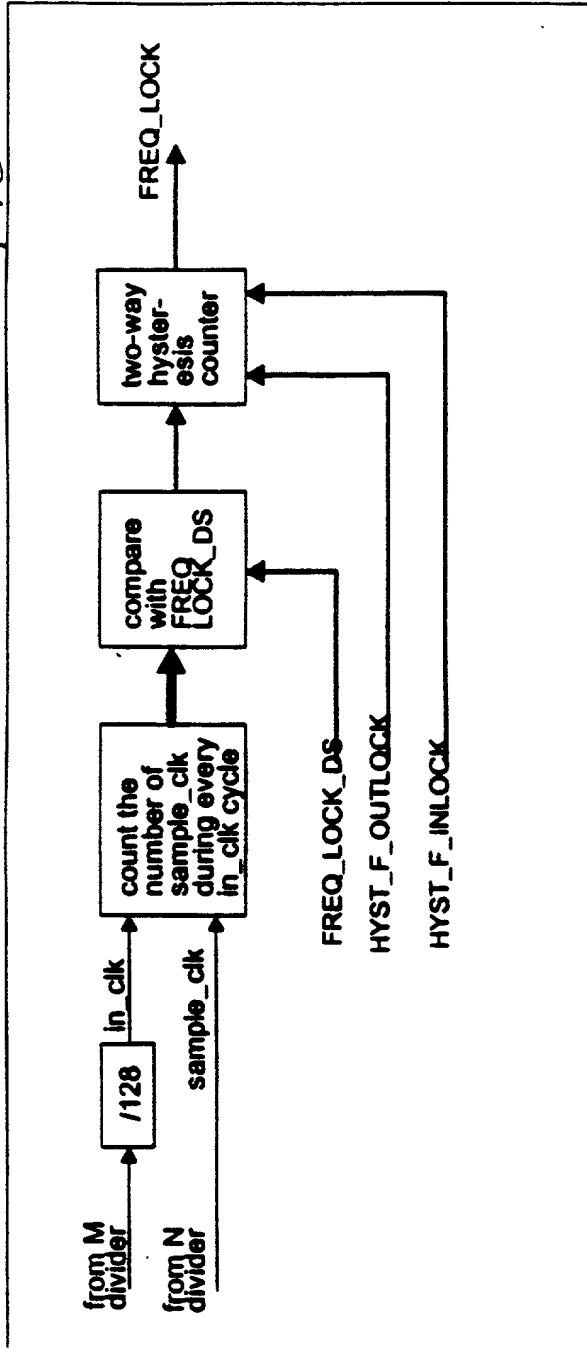


FIG. 11D



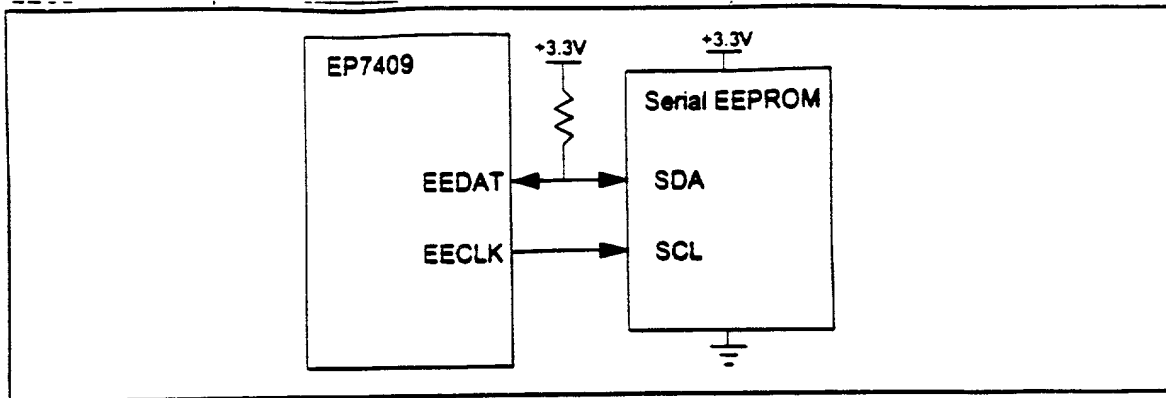


Fig. 12 A

Fig 12 B

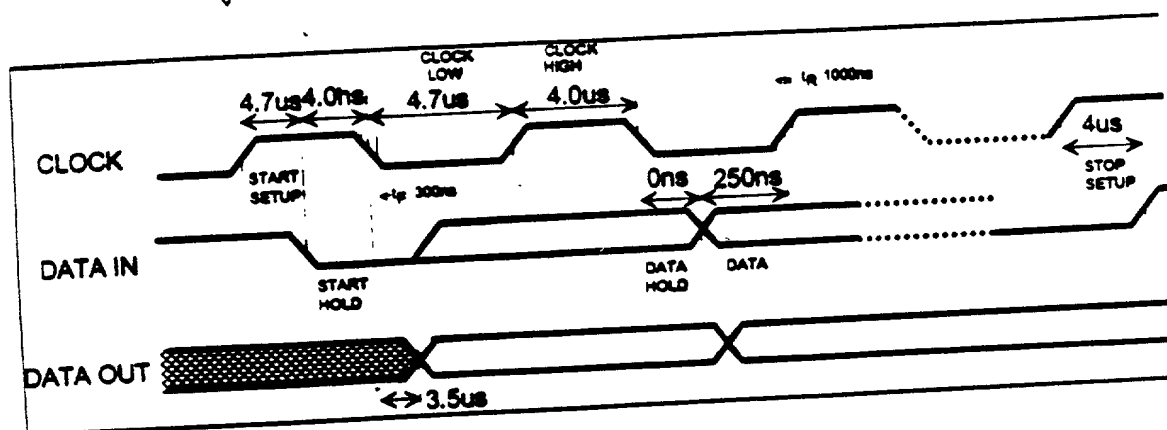
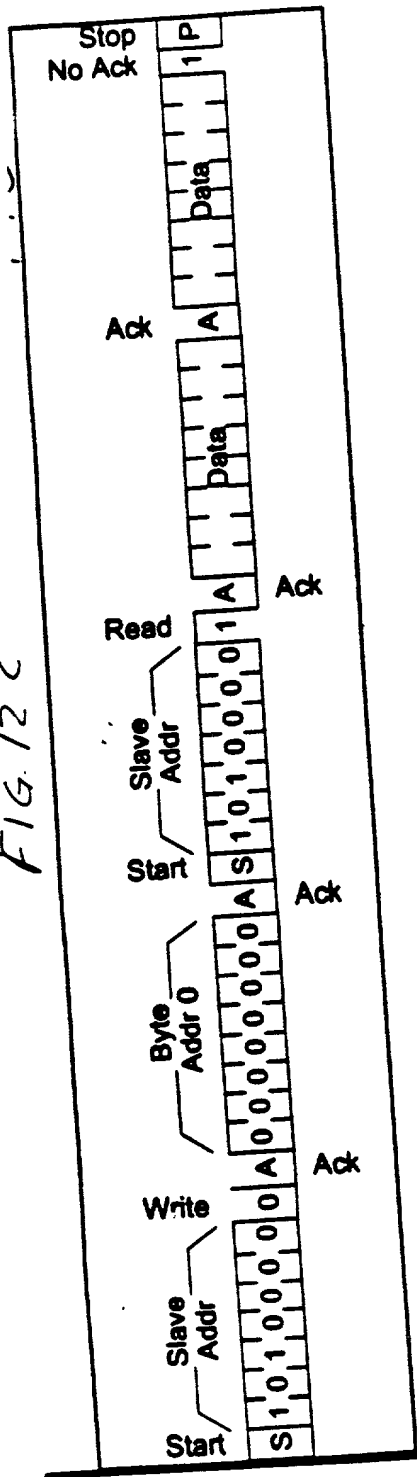


FIG. 12C



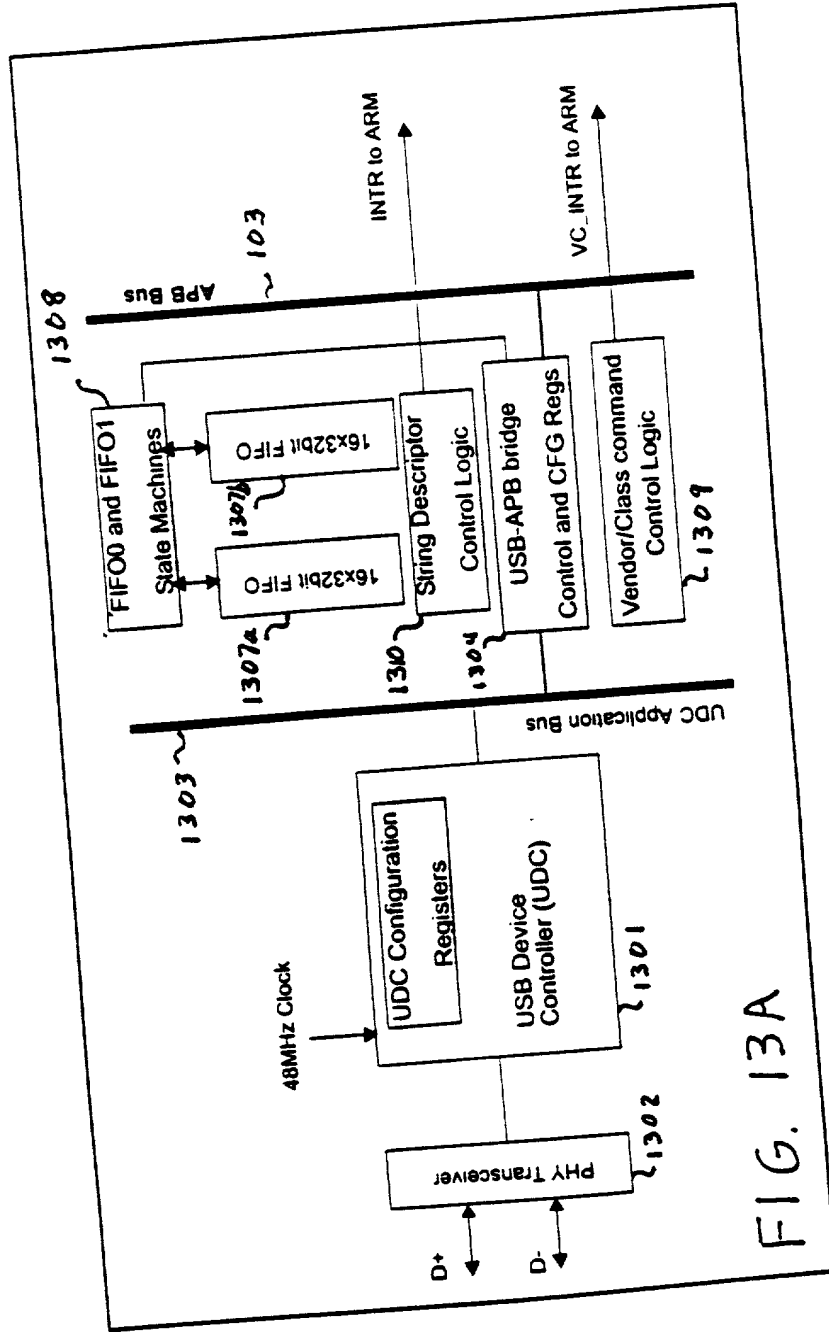


FIG. 13B

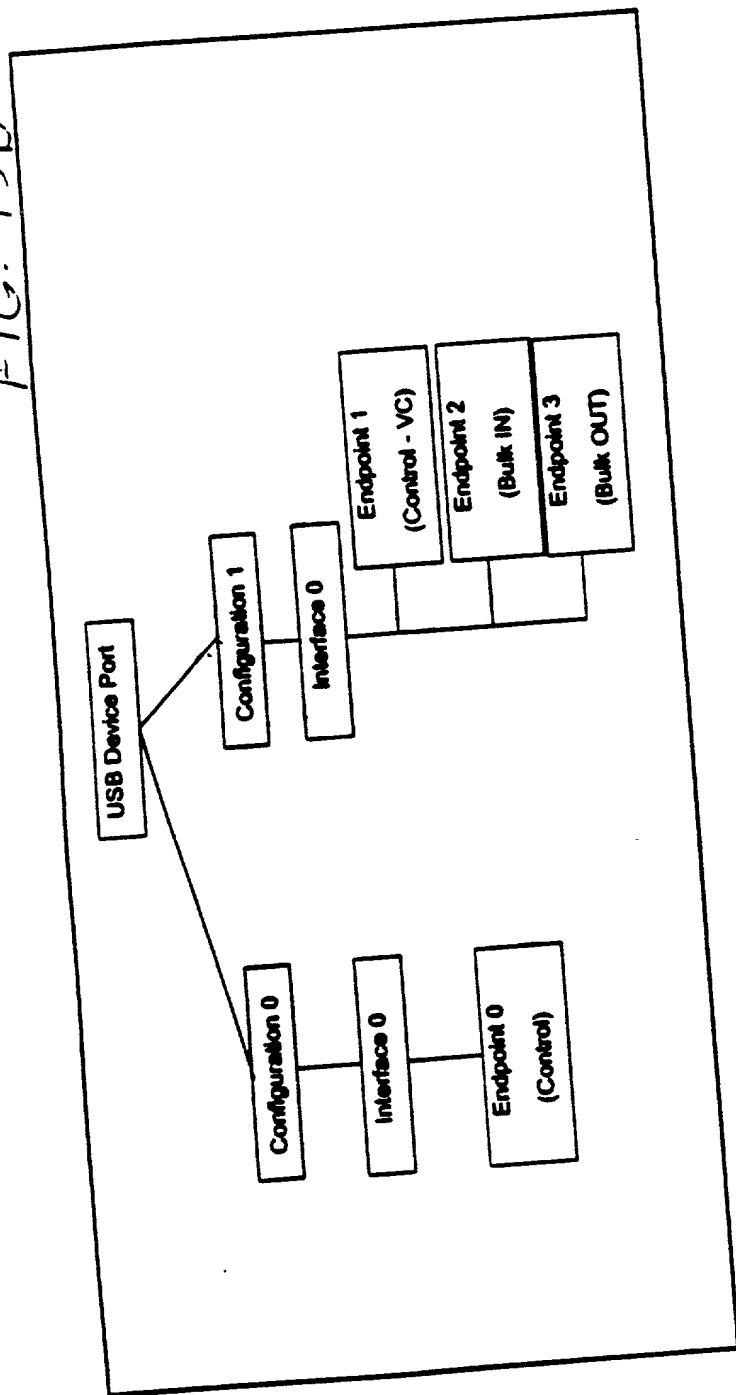


FIG. 14A

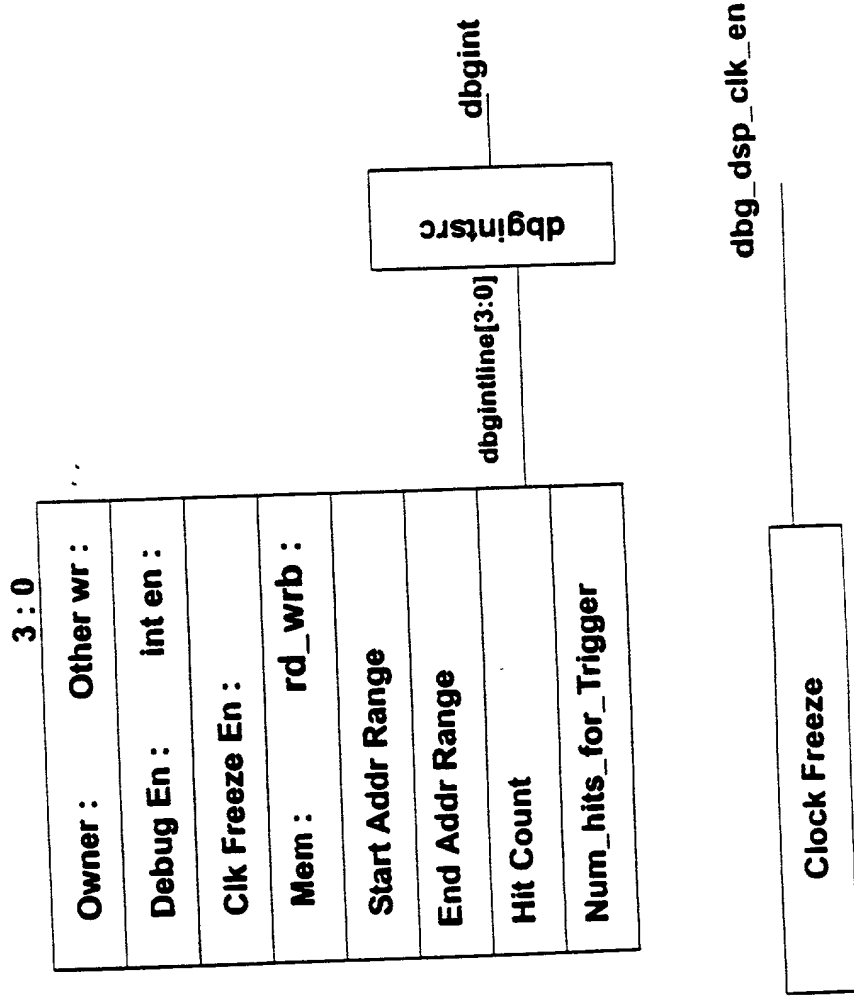


Fig. 14B

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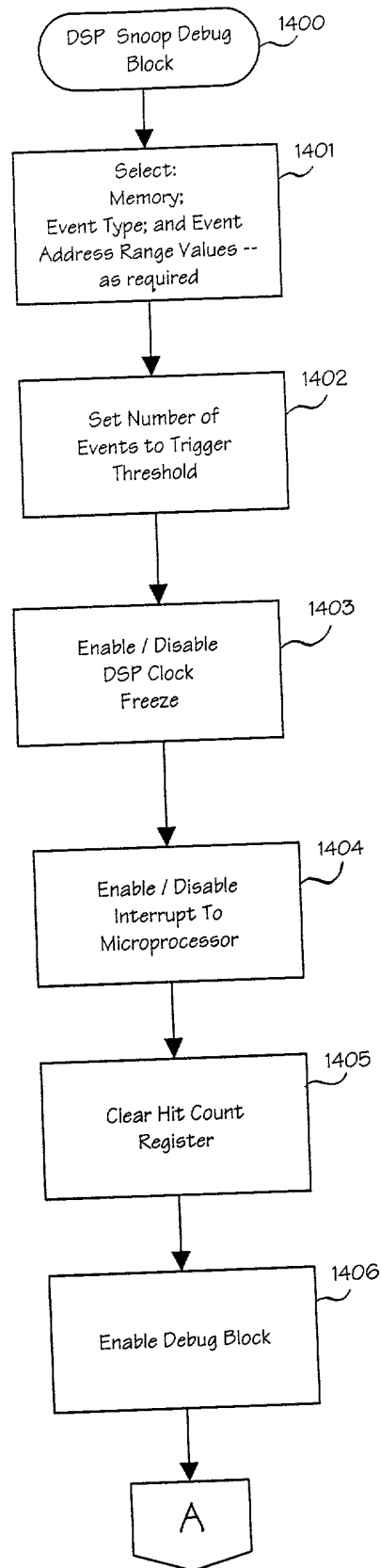


Fig 14B
Sheet 2 of 3

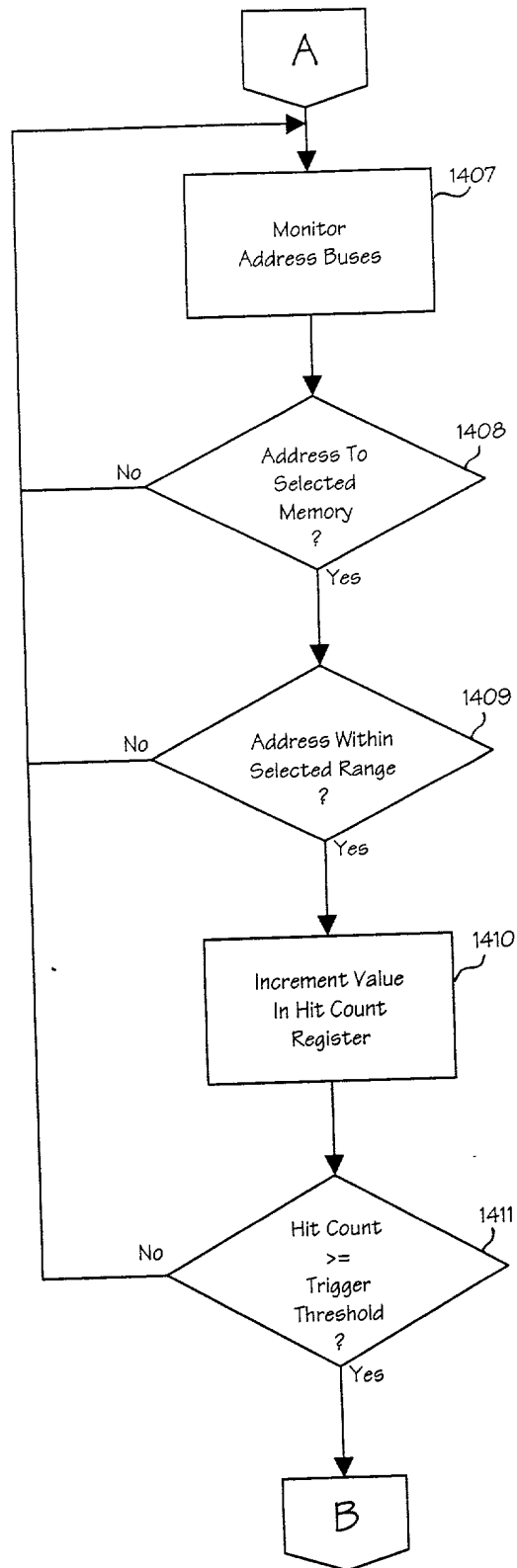
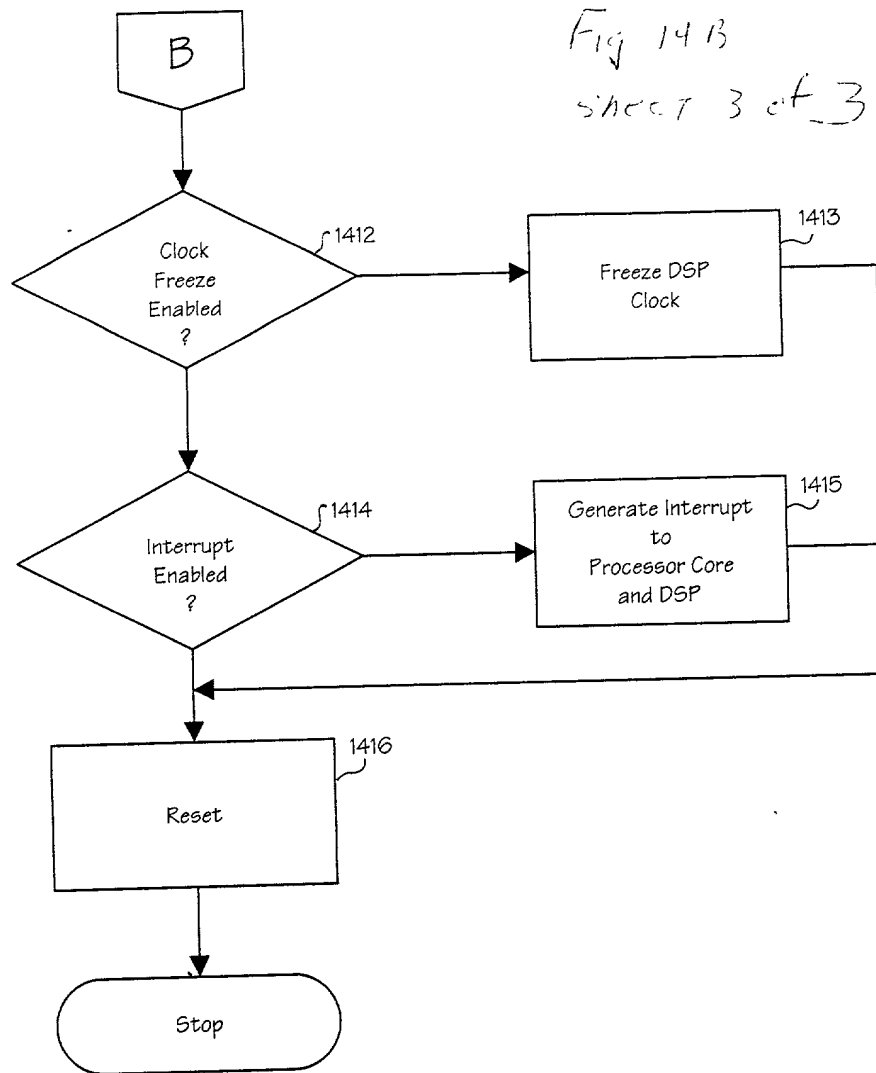


Fig 14B
sheet 3 of 3



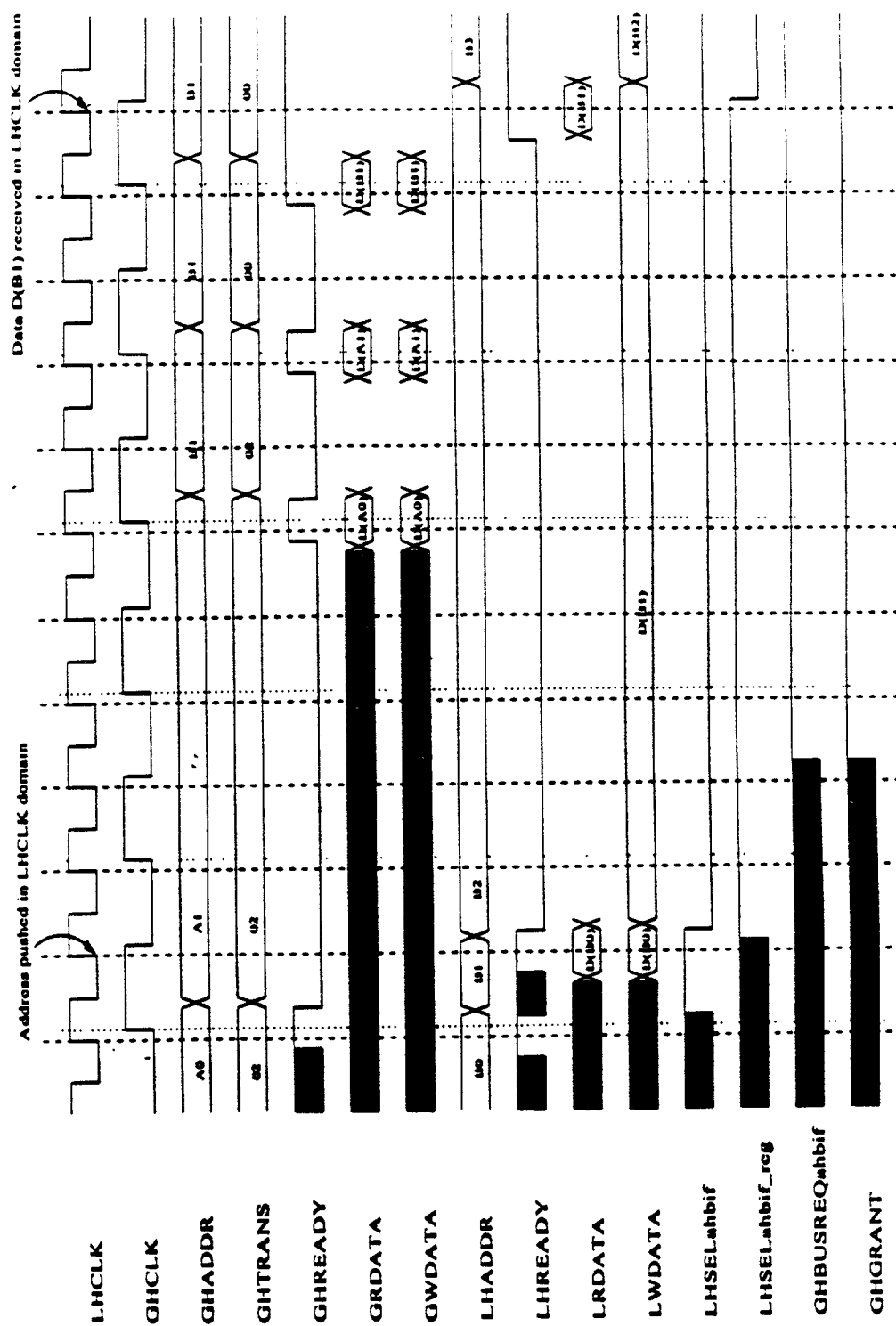
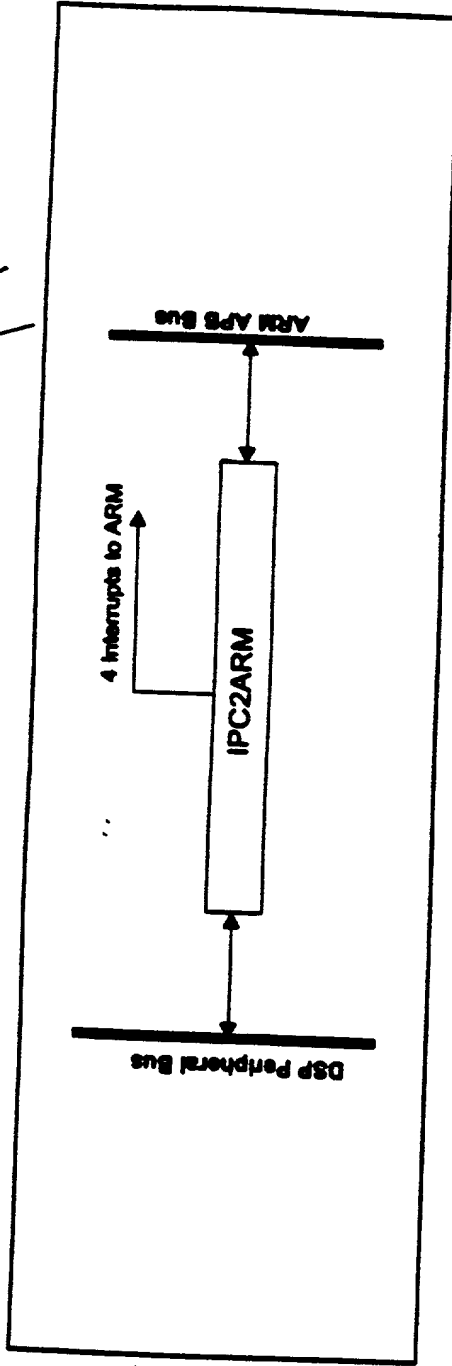


FIG. 2D

FIG. 15



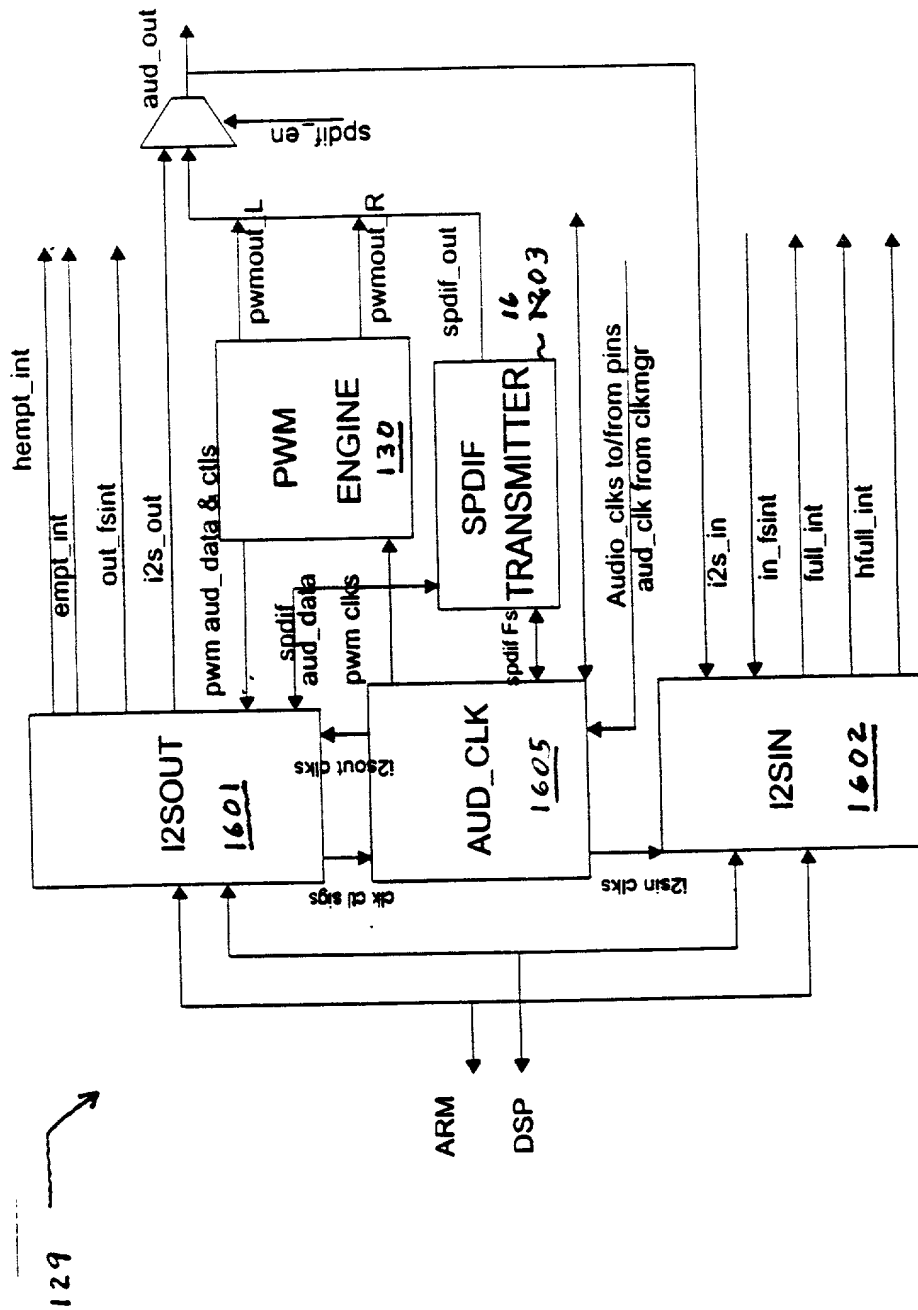


FIG. 16A

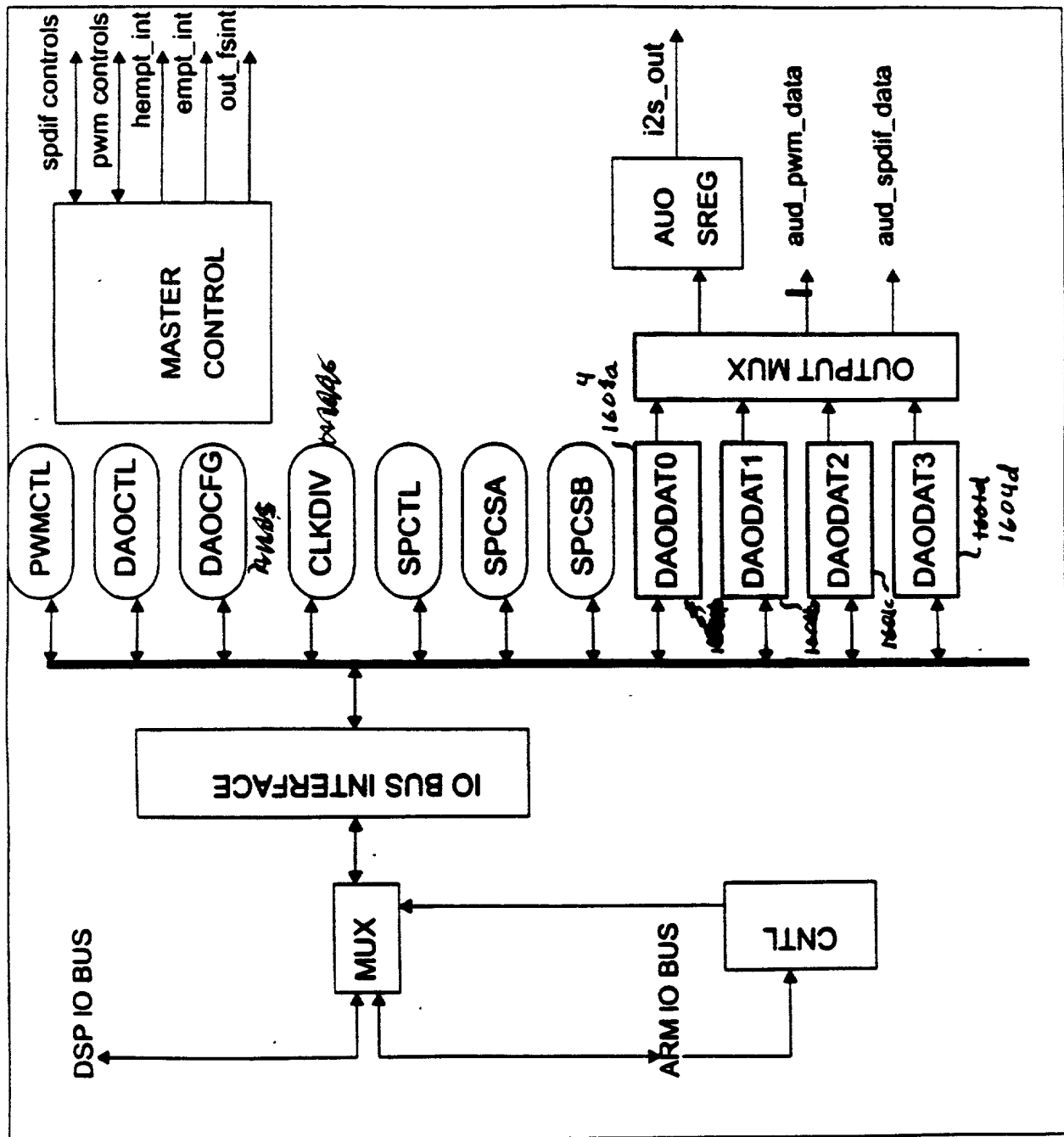


FIG. 16B

FIG. 16C

The following figure shows a typical output waveform.

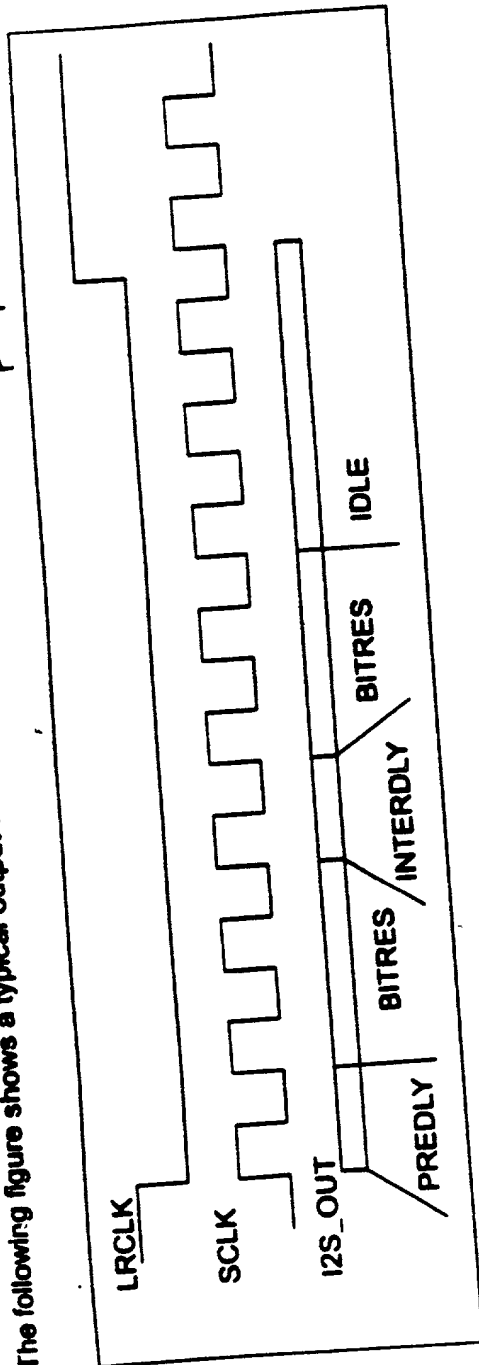


FIG. 16D

1602

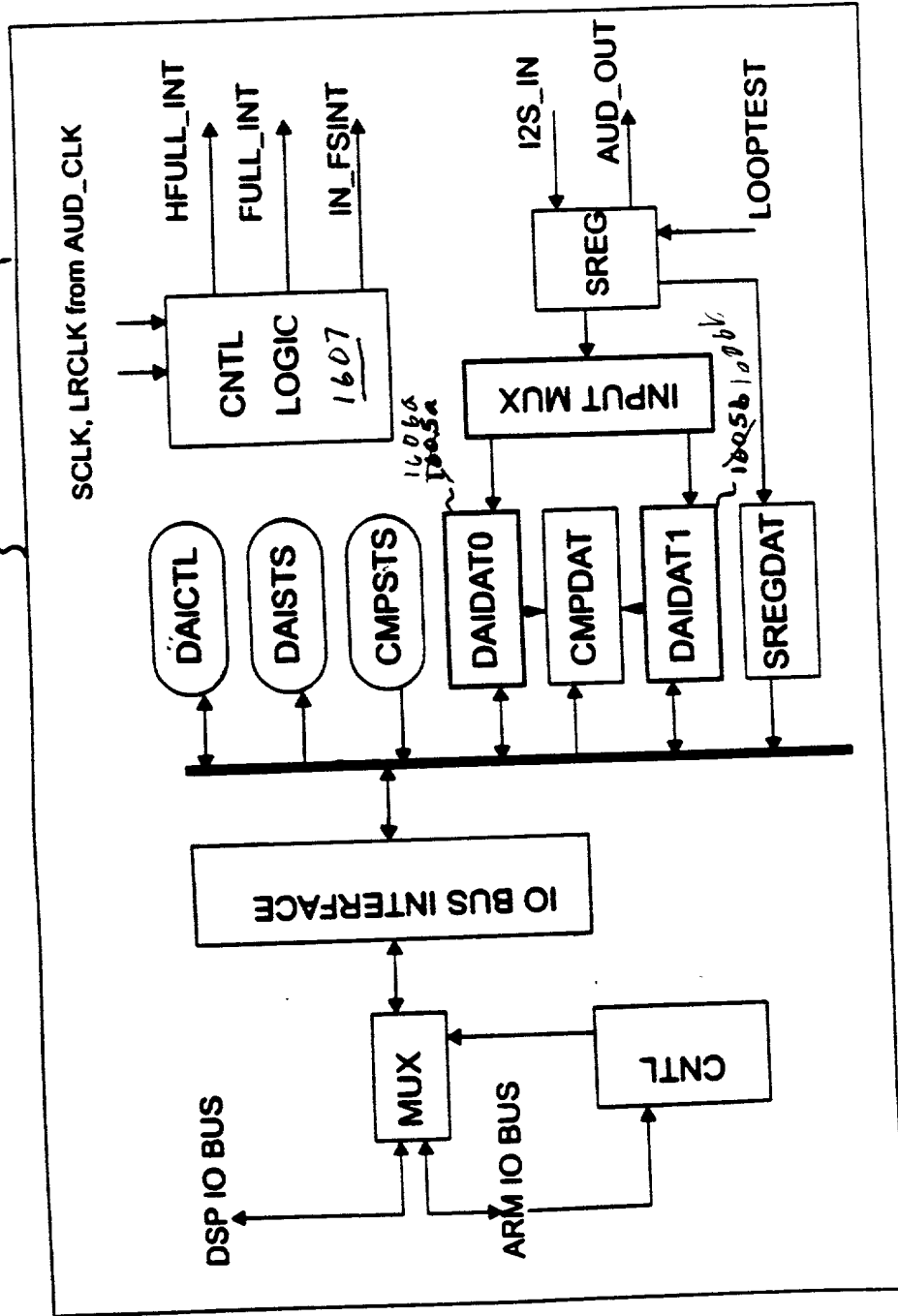


FIG. 17

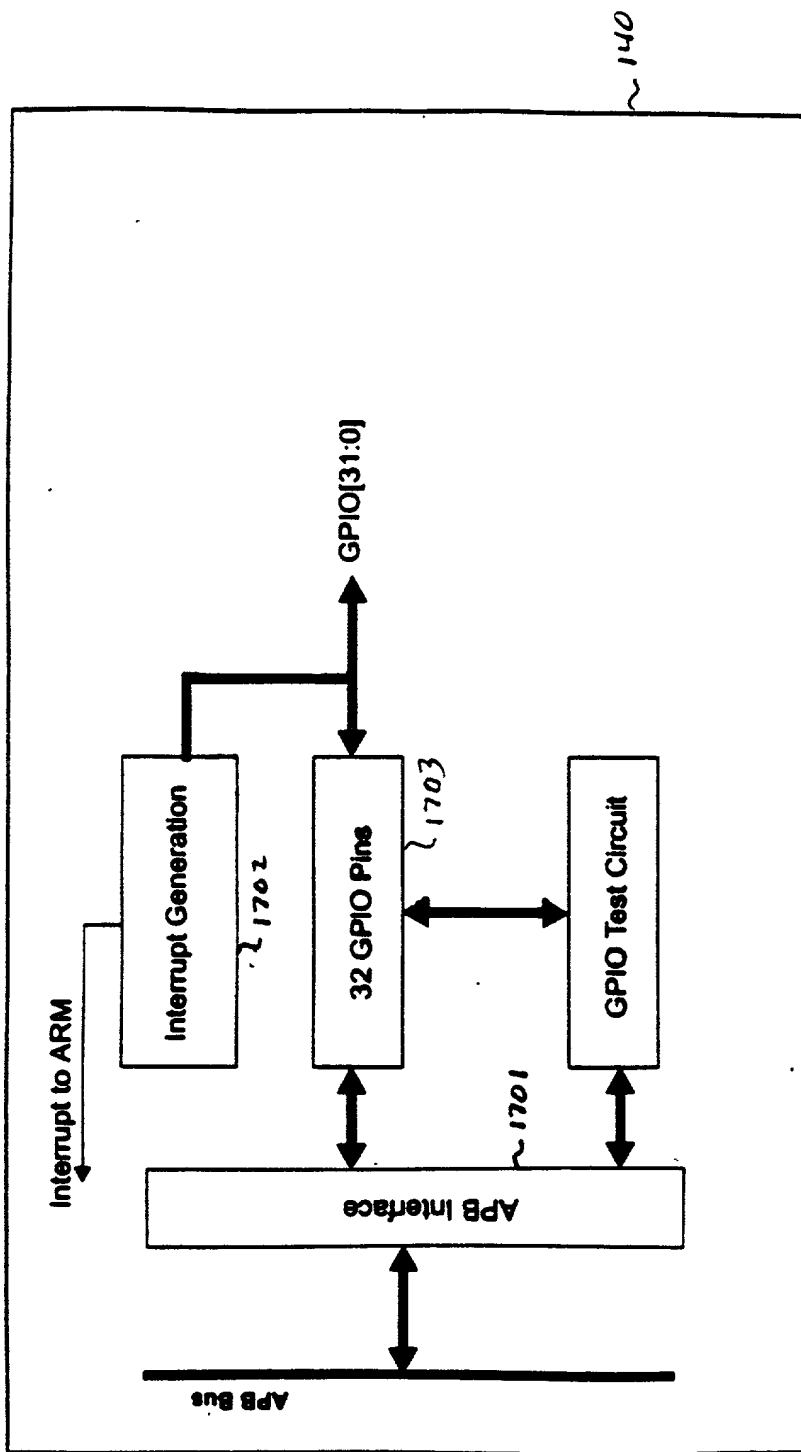


FIG. 18

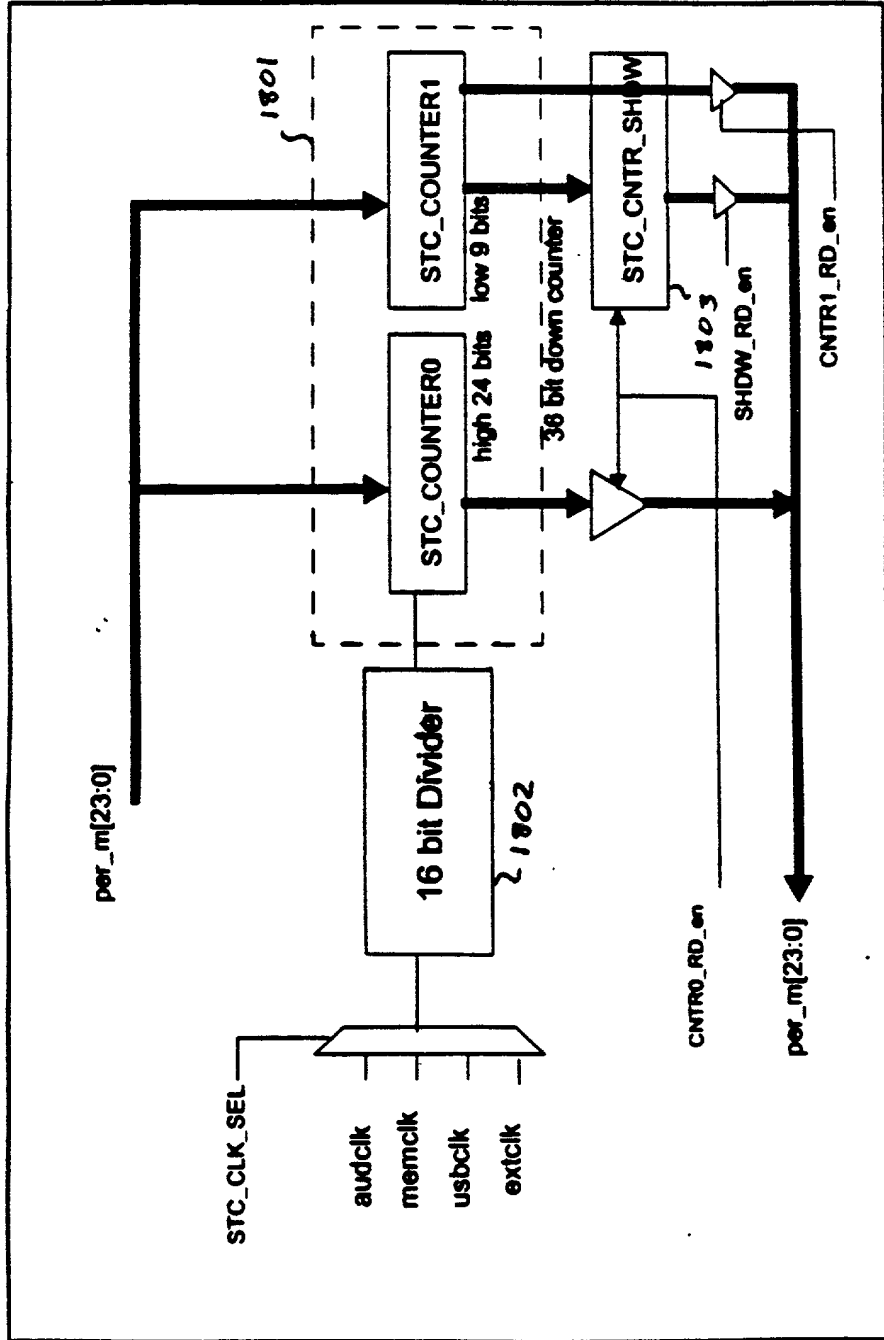


FIG. 19A

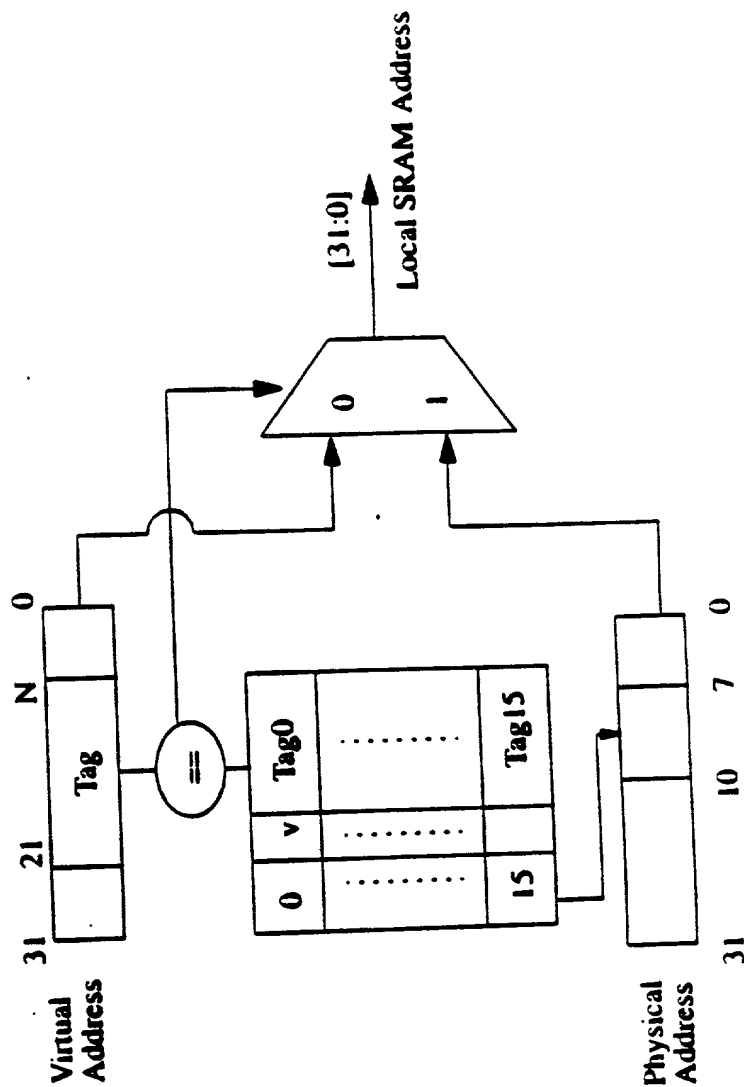
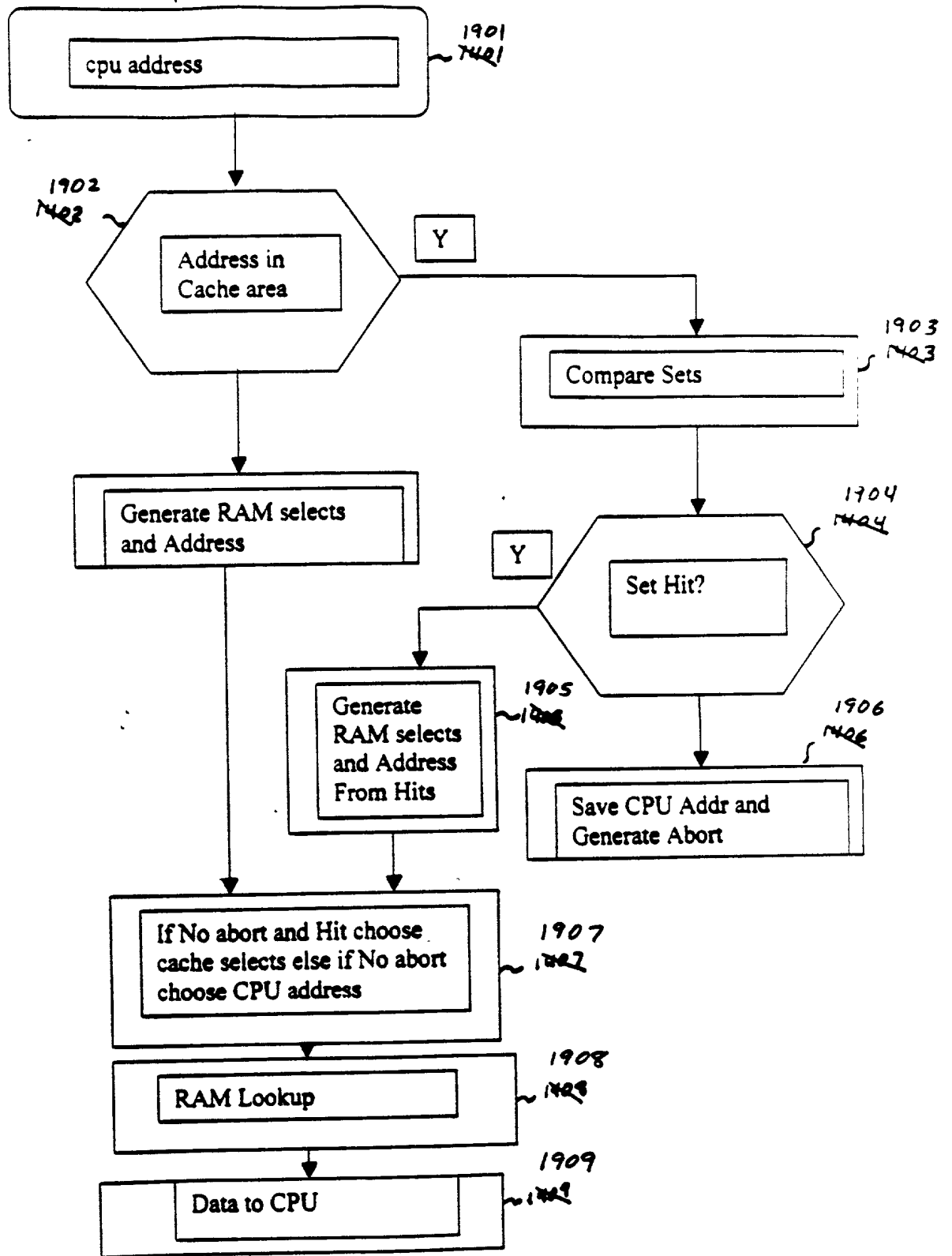


FIG 19B



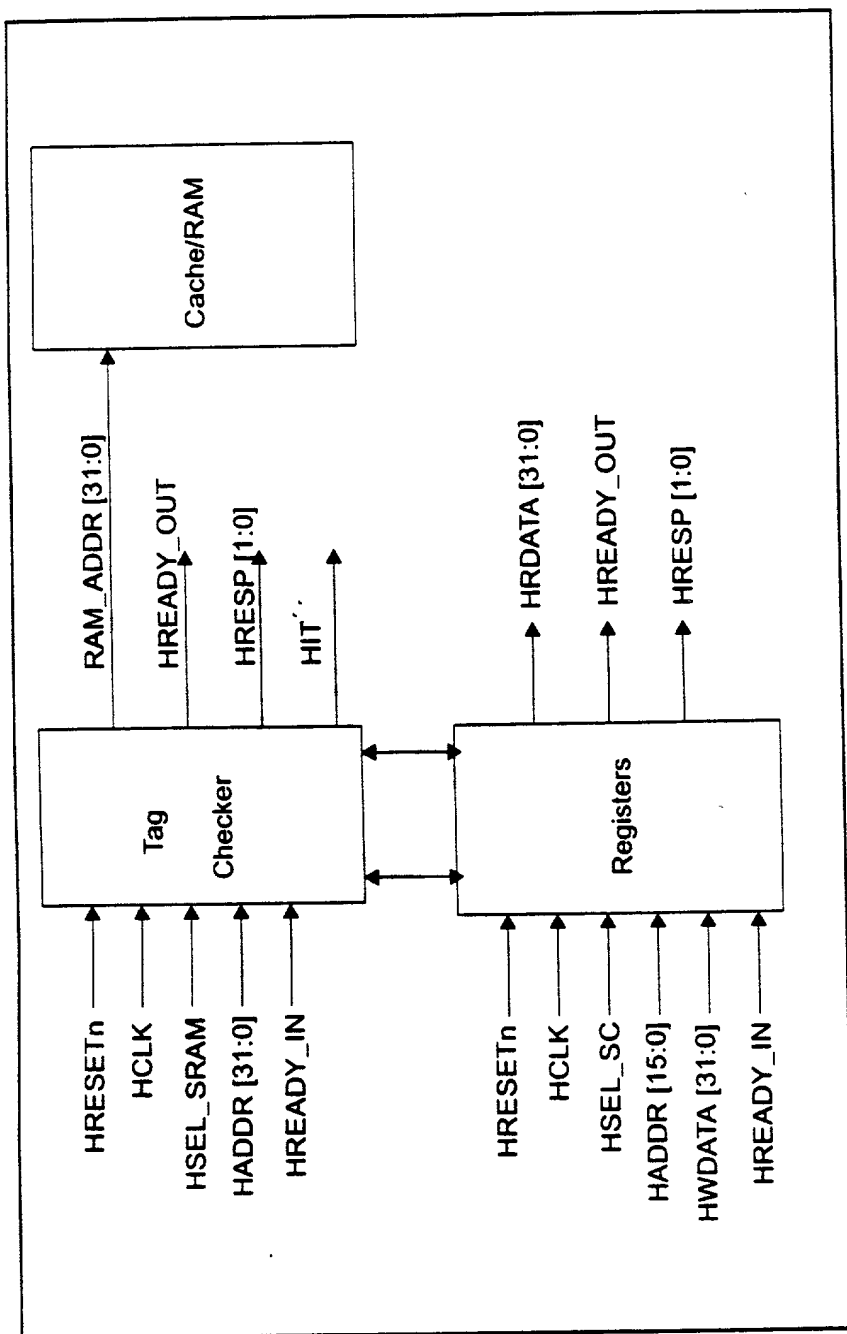


FIG. 19C

Fig. 20A

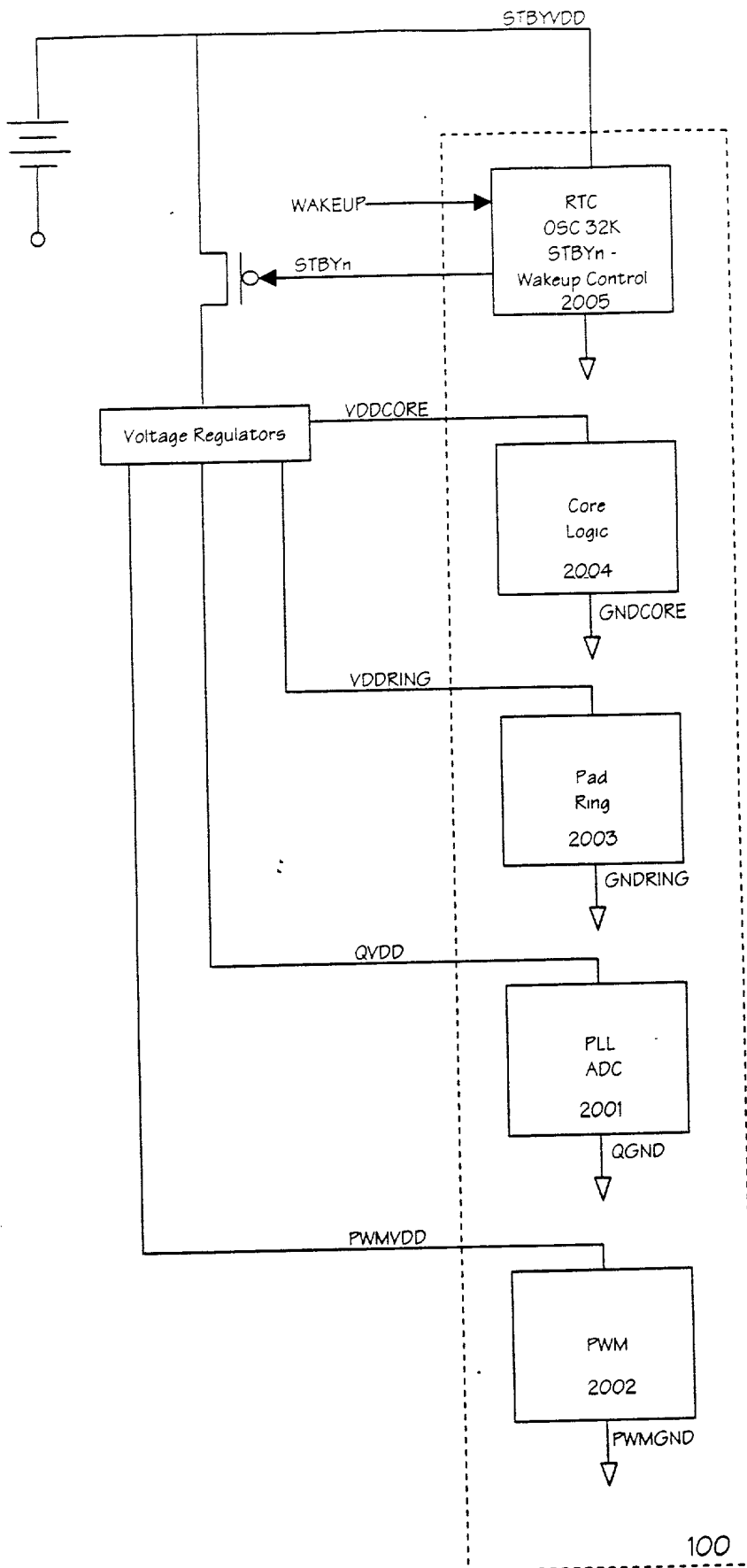


FIG. 20B

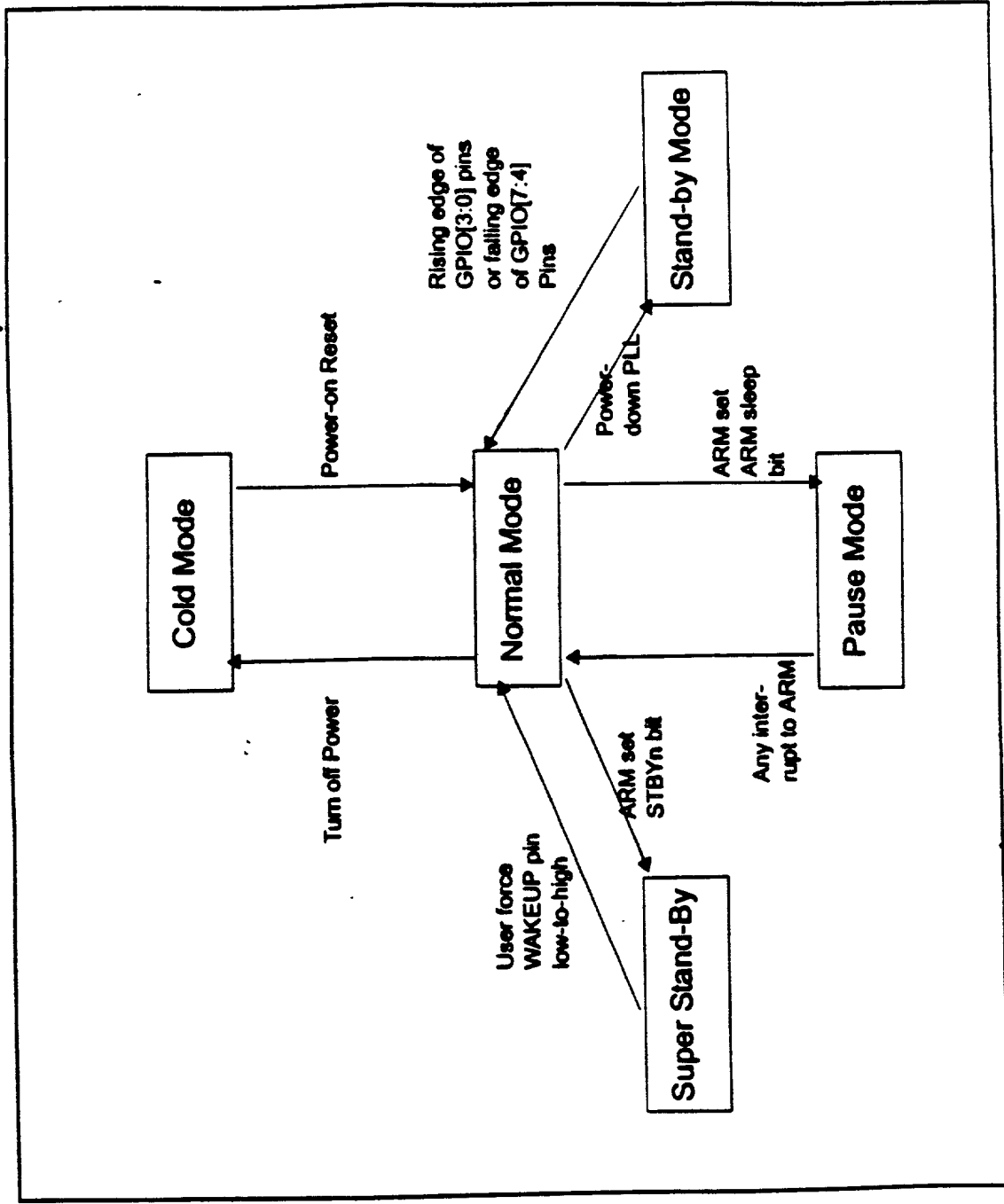


Fig. 20 C 5
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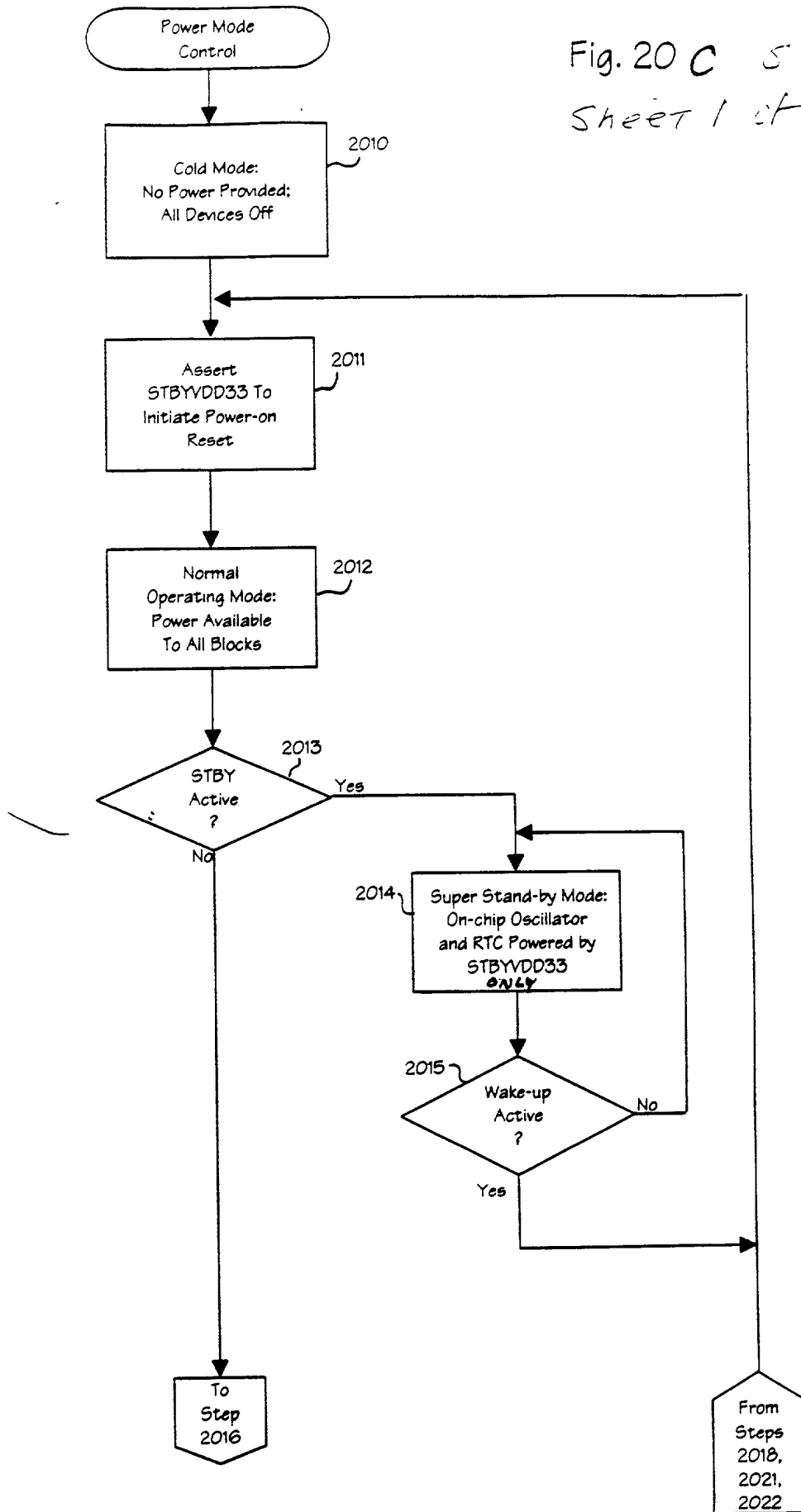
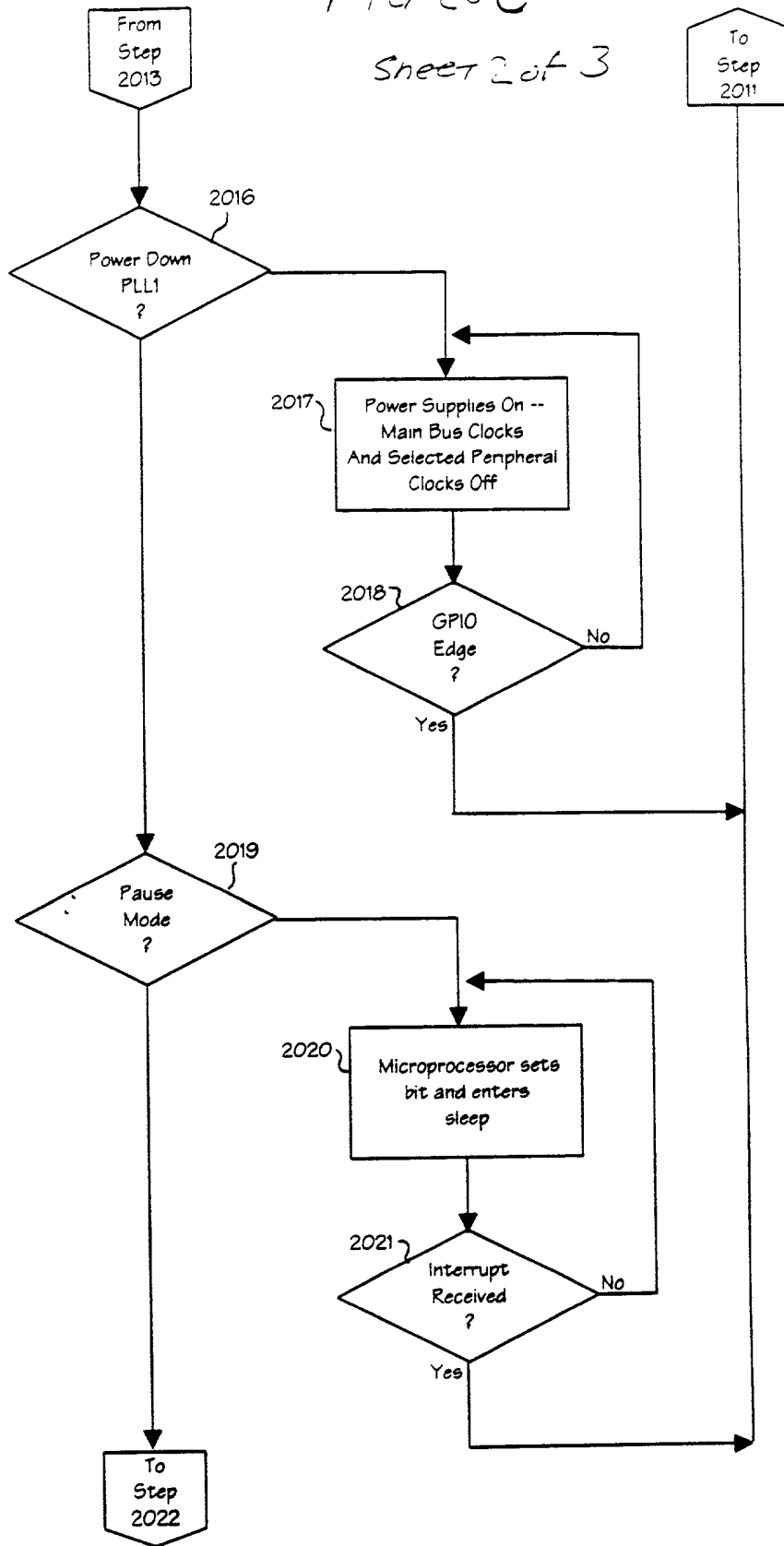


FIG 20C
Sheet 2 of 3



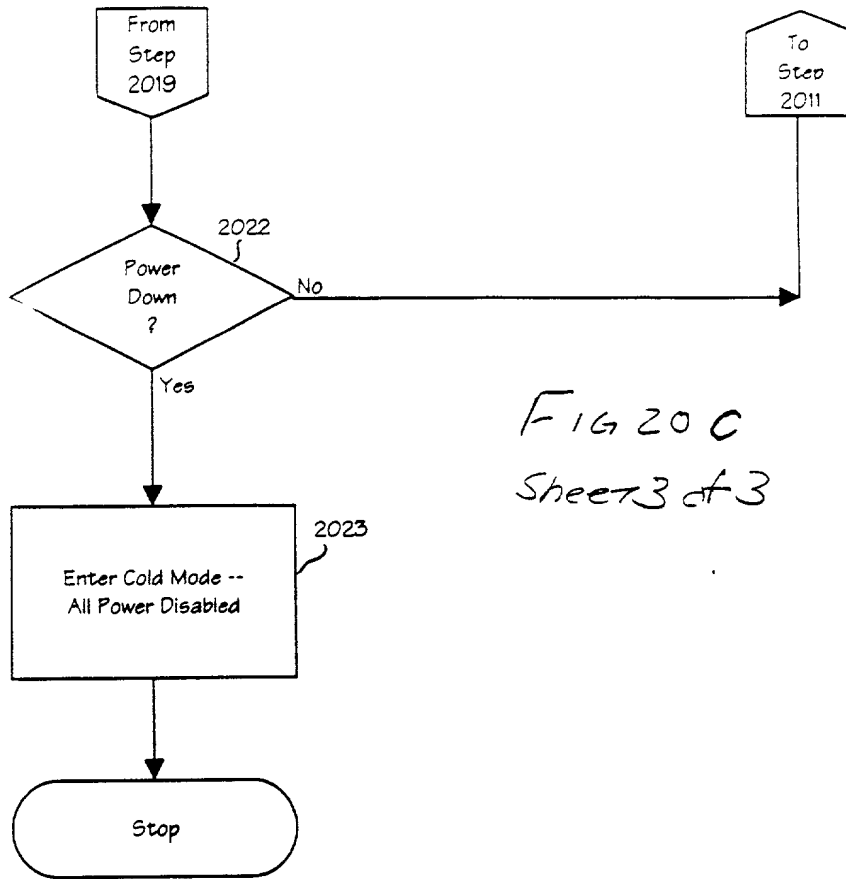


FIG 20C
Sheet 3 of 3

FIG 20C
Sheet 3 of 3

